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HYPERSONIC RESEARCH ENGINE PROJECT - PHASE II
CONTROL SYSTEM DEVELOPMENT
FOURTH INTERIM TECHNICAL DATA REPORT
DATA ITEM NO. 55-6.04
3 JANUARY THROUGH 2 APRIL 1968
NASA CONTRACT NO. NAS1-6666

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THE GARRETT CORPORATION
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REPORT NO. AP-68-3589

HYPERSONIC RESEARCH ENGINE PROJECT - PHASE IIA
CONTROL SYSTEM DEVELOPMENT
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PREPARED BY Engineering Staff

DATE May 22, 1968

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FOREWORD

This interim technical data report is submitted to the NASA Langley Research Center by the AiResearch Manufacturing Company, Los Angeles, California. The document was prepared in accordance with the guidelines established by Paragraph 6.3.3.2 of NASA Statement of Work L-4947-B.

Interim technical data reports are generated on a quarterly basis for major program tasks under the Hypersonic Research Engine (HRE) project. Upon completion of a given task effort, a final technical data report will be submitted.

This document presents a detailed technical discussion of the control system development for the period of 3 January through 2 April 1968.

ACKNOWLEDGMENTS

Acknowledgments for the completion of this document are herewith extended to the following contributors:

W. T. Curran, technical supervision and integration of report contents

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H. J. Bellamy, design of digital computer interface equipment

K. Hamilton, and B. Peretz, input/output system analog interface design

B. Paquette and H. Marthinussen, temperature control hardware and power supply design effort

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FIGURES (Continued)

FIGURES (Continued)

FIGURES (Continued)

LIST OF SYMBOLS

Symbol	Definition
T	Temperature
K	Thermal conductivity
A	Cross sectional area
X	Distance
$\dot{Q}_{in}$	Heat flow into hot skin
$\dot{Q}H_2$	Heat flow into coolant
Mw	Wall mass
Cpw	Wall specific heat
Tw	Wall temperature
$\dot{W}$	Coolant flow rate
Cp	Coolant specific heat
T_{out}	Coolant outlet temperature
T_{in}	Coolant inlet temperature
A_o	Hot skin area
A_t	Total hot skin and fin area
η_t	Fin efficiency
h_c	Convective heat transfer coefficient
TH_2 ave	Average coolant temperature
C_1	Coefficient for calculating T_{out}
C_2	Coefficient for calculating T_{out}
t_c	Computer time
τ	Real time
P	Servo set potentiometer
Q	Hand set potentiometer
ΔT_{out}	"Immediate" change in coolant outlet temperature
K	A constant
C_3	Coefficient for calculating "immediate" changes in T_{out}
$\dot{W}_{in}$	Coolant flow into lead circuit
$\dot{W}_{out}$	Coolant flow out of lead circuit
α	S-plane zero location
β	S-plane pole location

Symbol	Definition
IC	Lead circuit integrator initial condition
A	Amplifier
ϕ	Adjusted ratio of fuel to air
Q	Heat flow: Heat exchanger input
P	Pressure
W	Coolant flow
C_2	Valve constant
Pu	Upstream pressure
Av	Effective valve area
N	Ratio of choked flow to unchoked flow
PD	Downstream pressure
AV_{max}	Maximum valve area
AV*	Scaled valve area
T	Sampling period
t and s	Track and store
Eo	Output voltage
Ei	Input voltage
S	Laplace operator
γ	S-plane zero location
δ	S-plane pole location
Z	Sampled data operator
K	A gain
RC	Resistance X capacitance
α	Z-plane zero location
β	Z-plane pole location
γ	Z-plane zero location
δ	Z-plane pole location
D	S-plane zero location
E	S-plane pole location
F	S-plane pole location

LIST OF SYMBOLS (Continued)

Symbol	Definition
K_1	Coolant system gain
K_2	Temp control gain
K_3	Valve driver gain
T_{max}	Maximum temperature
ΔT	Temp rise across heat exchanger
D	Factor for calculating system gain
K	Open loop gain

1.0 SUMMARY

The Hypersonic Ramjet Engine (HRE) control system development has reached an advanced stage of breadboard hardware construction. Most of the existing circuitry has been functionally tested and some of the circuits have been tested over a wide range of temperatures. Test data, photographs, circuit diagrams, and descriptive material are included in Section 6.0.

Conceptual studies of failure modes have directly influenced the system and the detailed electronics design activities. An outline of the failure modes considerations is given in Section 4.0.

Some areas of analytical design are incomplete. The most significant of these are sections of the computer interface associated with auxiliary communications (teletype, GSE, and recorder) and a small portion of the analog output section.

Simulation studies are continuing, based on ground rules indicated in the second and third control system TDR's.

1.1 NONLINEAR ANALYSES

Simulation studies of the spike actuator dynamics were completed during this report period and are detailed in Section 5.0. Further work will be done on this subject if new requirements warrant.

Simulation of the fuel and temperature control functions has progressed to an operational stage in the analog computer facility. Heat exchanger characteristics have been dealt with in detail. Cooling system simulation has progressed to the point where usable design data is being provided for the temperature control electronics circuit development. A paper study of the hydrogen turbopump dynamics has begun.

1.2 DIGITAL COMPUTER

The Arma Micro D digital computer, its operating console, and the teletype equipment were delivered early in this reporting period. This equipment has seen extensive operation in the laboratory and is providing the necessary means for obtaining a practical working knowledge of the machine for both software and hardware engineering personnel. The equipment is being used for preliminary verification and testing of the software programs. Software activity is covered in detail in Para. 6.1.

1.3 POWER SUPPLY

The control system power requirements have been established, but minor variations will occur as design of the remaining electronics reaches its final stages. Conceptual design of the several power supply sections has been completed and breadboarding has begun. This activity is described in Para. 6.2, and the ground rules for further work on the power supply are outlined.

1.4 COMPUTER INTERFACE

Engineering effort in this area is divided into two sections which are closely related from a functional standpoint. Two two areas are the digital part of the interface (described in Para. 6.3.1) and the analog part of the interface (described in Para. 6.3.2). The distinction is made for the convenience in reporting the detail design activities, although some overlap exists in the functional descriptions.

Section 6.3 is devoted to conceptual circuit details and to circuit and hardware details for the breadboard activity. Components have been built and tested for a large part of the system interface. Except for the auxiliary communications, the digital section is very nearly complete.

1.5 TEMPERATURE CONTROL

Activity in this area has been somehwat constrained due to the scheduling of the simulation studies. However, considerable progress has been made as will be recognized by the extent of new hardware and circuit detail shown in Para. 6.4.

Simulation studies of the cooling system have advanced to the point where the temperature control concept is nearly complete.

2.0 PROBLEM STATEMENT

A control system is required to provide positive, safe control during ground and flight testing of a hydrogen-fueled, regeneratively cooled hypersonic ramjet engine. The control system must (1) schedule the fuel flow to the engine combustion chamber in accordance with programmed instructions to vary the fuel-to-air (equivalence) ratio as a function of certain flight parameters, (2) schedule the total fuel flow to the engine to provide adequate structural cooling, and (3) provide appropriate signals in response to indications of hazardous conditions. The control system must perform these functions over a wide range of environmental conditions consistent with ground testing and flight testing onboard the X-15-2 aircraft. The objective of the control system development program is the design and development of such an engine subsystem.

3.0 TOPICAL BACKGROUND

The engine design developed in accordance with the NASA-Langley Statement of Work L-4947-B must utilize supersonic combustion at freestream Mach numbers from 6 to 8. In the freestream Mach number range from 3 to 6, the combustion code may be subsonic to yield the best performance. In addition, means must be provided for inlet flow start and initiation of combustion, including at least one restart, after engine shutoff at any speed from Mach 3 to 8. The control system must (1) schedule engine fuel flow, in accordance with the computer freestream Mach number; and (2) establish, transfer, and maintain the desired combustion mode consistent with programmed instructions.

To achieve reliable operation over the intended hypersonic flight regime, hydrogen fuel must regeneratively cool major portions of the ramjet engine structure. The hydrogen fuel/coolant flow must be adequate under all engine operating and nonoperating conditions to limit metal temperatures and temperature differences compatible with sound structural design. In some engine nonoperating conditions and some operating conditions, fuel flow is sufficient to cool the engine combustor. The fuel system, therefore, will include an overboard dump valve to permit fuel flow in excess of engine combustion requirements. The control system must sense the critical structural temperatures and initiate and maintain coolant flow as necessary.

To permit operation of the engine over the Mach number range from 3 to 8, the inlet spike must be translated to various positions. The control system must compute the freestream Mach number based on sensed flight parameters, determine the appropriate spike position, and signal the spike actuation system.

The control system will be housed within the engine nozzle cavity. Accordingly, size and packaging limitations govern the design. Further, the need for access and replacement of components in the field must be kept to a minimum, consistent with the research nature of the program.

4.0 OVERALL APPROACH

The overall approach follows the same general lines indicated in the second and third control system (References 4-1 and 4-2). Section 4 is primarily devoted to further explanations of and refinements to the control system configuration as related in the referenced documents. New material on system monitoring concepts is included.

In cases where there is disagreement, statements in the later TDR's take precedence over earlier TDR's. Specific reference will be found in the text relating such changes to previous conditions.

4.1 CONTROL SYSTEM OPERATION

The control system has two prime functions: (1) to control the inlet geometry and the fuel flow to the combustors, and (2) to provide safe operation and automatic precautionary control as conditions dictate.

In general, the control system operates automatically under the control of stored program data. It receives various stimuli from sensors in the system and only in a few instances will it be subject to the influence of manual discrete commands

4.1.1 Engine Control Sequence Stimuli

Control system activity depends only on the presence of electrical power. It will tolerate temporary power lapses that will occur during the switching of sources (e.g., ground to B-52, to X-15A-2) prior to launch. The first control mode switching will occur automatically in response to a discrete signal identified as the predrop signal. This mode change should be executed prior to the final commitment to launch the X-15A-2, so that the switchover is verified by the self-test routine.

The predrop signal puts the engine control program into a "ready" status. Prior to this, the system will be functioning in a self-check mode which includes system degradation tests. The level of monitoring which occurs before and after the predrop signal is more fully described in Section 4.4 under monitoring concepts. After the predrop signal, the system will be operating in its primary mode, but still without the ability to mechanically control engine functions. This constraint exists because the servovalves are inoperative until pneumatic and hydraulic pressures are supplied.

During high Mach number flights, hydrogen flow will be required for cooling prior to any requirements for fuel injection. A selected temperature measurement will automatically trigger initiation of the helium purge and startup of the hydrogen cooling flow. Under these conditions, if conservation of nitrogen is a problem, the nitrogen gas supply need not be initiated until the pilot switch is turned on. The inference here is that a short delay in startup sequence will be experienced until the spike actuator hydraulic pressure comes up to operating level. The starting sequence will then follow the routine indicated in Figure 4.3-10, page 4.23 of Reference 4-1. Power for the spike hydraulic system and for the fuel injector valves is supplied from the nitrogen pressure.

During some low Mach number flights, hydrogen will not be required for cooling prior to startup. The initiation of the purge and hydrogen flow will cause a short delay in the startup activity; this allows the turbopump to reach an acceptable operating configuration prior to the demand for fuel delivery. Initiation of the nitrogen gas supply pressures will be programmed at the same time as the purge.

The primary manual control input is the pilot's switch, which, when switched "on," introduces a control mode change during the X-15A-2 flight phase. This interval is identified as the "HRE Test" in the program sequence, as described in Reference 4-2, Table I, page 6. An ignition "on" signal will be provided automatically by the control system. The conditions and duration of the ignition interval have not yet been defined. During normal operating conditions, at the end of the HRE test interval, the pilot must turn the switch off manually. This action will close the fuel injectors, shut off ignition, and close the engine inlet. The temperature control will continue to operate the cooling system. A programmed time limit for the test can be provided as a shutdown safety condition. If any of the engine warning signals appear (e.g. low LH_2, N_2, He) the engine will be shutdown automatically even though the pilot switch is "on," and a normal cooling configuration will proceed. The cooling system will be shutdown automatically when descent conditions reach a sufficiently low heat input configuration and indicate a low enough temperature for shutdown. In either case, all control system power should be turned off to minimize any temperature soakup when cooling becomes inactive during descent. Implementation of this power shutdown will be reviewed in terms of functional safety.

Many of the mode changing stimuli are derived from data being processed in the digital computer during its control computations. Other discrete signals used are inputs specifically intended for monitoring and mode control. A list of the various discrete signals used in the computer program is given in Table 4.1-1.

4.1.2 Valve Operating Configurations

Clarification of the operation of the control system electronics requires examination of operating configurations of the nine control valves. For fail-safety reasons, all valves will go hardover when electrical power is removed from the valve drivers. The coolant valves and the dump valve will open. The fuel valves will close and the inlet will be driven to the closed position.

TABLE 4.1-1

INPUT/OUTPUT DISCRETE SIGNALS

Input			Output			
Pilot switch		1	Ignition			1
Gas supplies:	Low LH_2	1	Gas supply activation:	Purge He/LH_2		2
(Monitoring)	Low N_2	1		Squib N_2		2
	Low He	1		Valve supply He		1
Predrop signal		1	Monitoring:	Go/No-Go (Warning Light)		1
				Shutdown		1
				Fire		1
	Total	5			Total	9

4.1.2.1 Spike Actuator Valve

The spike control valve acts as a proportional device when the LVDT position signal is within ±0.6 in. of the position command. When the position error exceeds 0.6 in., the valve will go wide open in the direction corresponding to error signal polarity. With electrical power absent (valve driver power removed) and hydraulic pressure normal, the actuator will drive the inlet to the closed position due to a mechanical bias in the control valve. With hydraulic pressure absent, the actuator will not respond to electrical drive signals.

4.1.2.2 Cooling System Valves

The coolant regulator valves (CRV's) and the dump valve function as proportional control devices for temperature intervals near the reference limits. With the electrical power off and gas pressure (H_2) present, the valve areas are at a maximum for all five valves. With gas pressure absent the valves will go wide open irrespective of electrical drive conditions. The startup conditioning and valve action is reviewed in Para. 4.1.3 in the discussion of hydrogen flow initiation.

4.1.2.3 Fuel Control Valves

The three fuel control valves (FCV's) function as proportional control devices in response to the fuel flow and distribution commands from the digital program. With electrical power absent and gas pressure (N_2) present, the fuel valves will close. If the nitrogen supply pressure is absent, the valves will close regardless of electrical drive conditions.

4.1.3 Initiation of Hydrogen Flow

There are two separate configurations for initiation of hydrogen flow. One is associated with the higher Mach number flights and requires hydrogen flow for engine cooling in advance of requirements for fuel injection. The other configuration at low Mach number demands hydrogen for fuel injection only. In either case, the helium purge cycle precedes the input of hydrogen to the system plumbing and is executed by a time interval control.

4.1.3.1 Higher Mach Number Flights

The higher Mach number conditions generally will demand that cooling be started at a predetermined Mach number or temperature limit. Conditions as determined by the data being processed in the digital computer will be tested for operating limits. When the governing limit is reached, the purge cycle will be initiated. Under these conditions there will be no injector flow and the dump valve must be opened.

Initially the coolant flow valves and the dump valve will all be wide open due to an absence of gas pressure across the pneumatic section of the servo valves.

It is assumed that all temperature measurements for the temperature control will still be below their limiting values and that the electrical commands to close all the valves are present. Therefore, unless some special provision is made, when the hydrogen flow builds up there will be a tendency for the cooling valves and the dump valve to close. Using established minimum valve areas and a directly applied small overdrive signal to the dump valve, the cooling system can be sustained in a fully operational condition at a relatively low level of cooling flow. In this condition, normal operation will develop as temperature demands supersede the residual low-level cooling flow.

The next transition occurs when the inlet opens but the engine is still not lit. Some redistribution of flow will occur and the overall heat load will rise resulting in a normal increase in dump flow.

A third phase follows as fuel delivery to the injectors is initiated. As injector flow increases, dump flow should decrease proportionally. Computer command dictates injector flow and the dump flow decrease will be in response to the temperature decrease which occurs temporarily because of the total flow transient. A question arises concerning the effects of this transient (in terms of plenum pressure) on the stability of the rate of fuel delivery to the injectors.

This potentially destabilizing influence can be handled in two ways. One method is to control the rate at which the injector valves open. A nominal interval would be about 1/2 sec according to present estimates. Another approach is to arbitrarily shut the dump valve when the injectors are opened, thus minimizing the change in total flow.

As the simulation studies progress, the system reaction to injector flow initiation will be examined to determine if a real problem exists. In the meantime, sufficient flexibility is being built into the breadboard circuits to provide communication between the computer and the temperature control so that the methods proposed above can be implemented as required.

4.1.3.2 Low Mach Number Flights

Some low Mach number tests will require that fuel injection begin prior to any demand for system cooling. The engine will be brought to the ready condition and tests begun in the manner previously indicated in Para. 4.1.1.

The procedure is the same as for the initial conditions described, in Para. 4.1.3.1 above. Since a cooler inlet starts easily, it may be desirable to overcool the inlet slightly by making the initial dump valve overdrive signal larger than the nominal minimum flow requirement.

The transition to the required injector flow should be straightforward with the injector valve signal and the removal of the dump valve signal timed to minimize the total flow transient.

4.1.4 Cooling Considerations Related to Engine Shutdown

The transition between combustor cutoff and pure cooling configuration in the presence of high heat loads will probably require some anticipation to maintain stable flow conditions. The necessity will be determined in a later stage of the simulation studies.

The anticipation would consist of a forced opening of the dump valve as the injectors are shut down and then a transition to normal operation by the temperature control. A similar procedure will apply to an unstart, with the restarting sequence generated appropriate to the existing flight conditions as previously indicated.

4.2 SYSTEM DESCRIPTION

The control system configuration is essentially the same as outlined in previous TDR's. Changes at the circuit detail level are covered in Section 6 of this report. There are, however, details related to mechanization of engine startup and monitoring functions which will be presented below. The two functional subsystems discussed are representative of the approach employed in the control system for monitoring analog interface elements.

4.2.1 Spike Actuator Mechanization

The functional block diagram shown in Figure 4.2-1 is the analog output section that controls the inlet geometry. This is the configuration indicated in Figure 4, Page 11 of Reference 4-2. The command is generated by the digital computer and the loop is closed externally. This approach provides tight loop closure with a simple feedback circuit. The dynamics response for this configuration is reviewed in detail in Section 5.1 of this report. The ram rate transducer was eliminated as a result of the simulation study.

Two monitored items are indicated in Figure 4.2-1. One is the drive current to the torque motor; the other is the LVDT output. The signal from the LVDT can be compared with the computer-generated command. The failure modes and safety checks on this control will be presented in complete form in the next quarterly report.

Position data from the LVDT is input to the computer for the additional purpose of recording it for later data reduction on air mass flow calculations.

4.2.2 Temperature Control Mechanization

Figure 4.2-2 shows the information flow for the basic temperature control and its lines of communication with the computer interface. These lines serve the purposes of engine startup control and monitoring. Startup is dictated by the digital program and will follow the methods outlined in Para. 4.1. The monitoring is discussed generally in Para. 4.4.

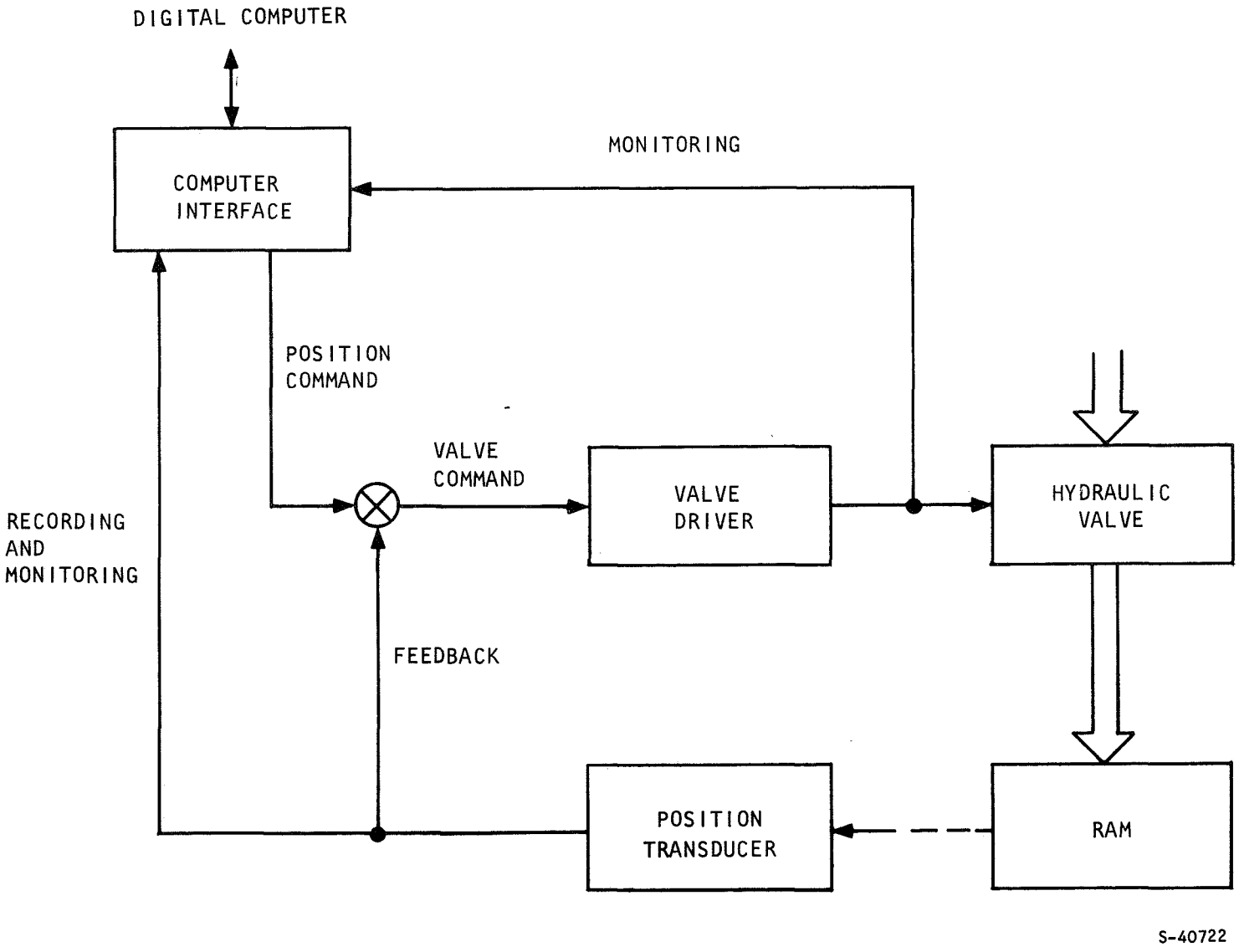

Figure 4.2-1. Analog Output Section, Spike Actuator

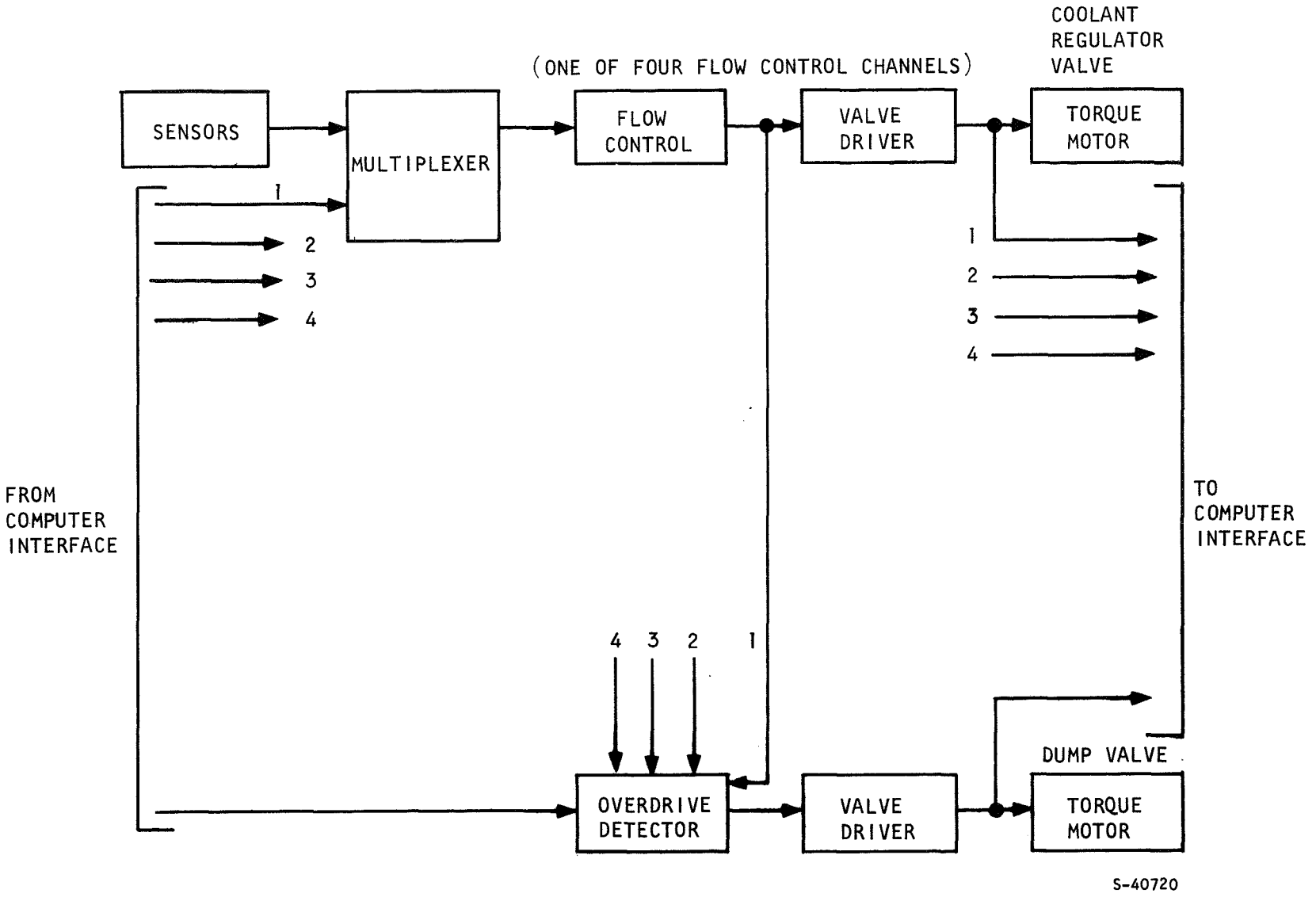

Figure 4.2-2. Temperature Control Block Diagram

The inputs from the computer to each flow channel multiplexer and to the dump valve overdrive detector will permit any combination of valve area setting. The output current to each torque motor is sensed and the data is then checked in the digital computer to determine if the temperature control responded properly. During ground testing when gas pressure is available, fluid flow can be measured and compared with torque motor current as a check on the hydro-mechanical elements of the valves.

4.2.3 Fuel Control Mechanization

The computer outputs valve position (valve area) commands to the respective holding amplifiers which, in turn, present continuous electrical signals to the valve drivers. The loop is controlled through the digital computer as a function of combustor limits or on total fuel mass flow as indicated in the second TDR.

The drive current to the fuel valve torque motors is transmitted to the computer interface for monitoring in the same way as previously indicated for the other control valves.

4.3 TRANSDUCER STUDIES

In the third TDR, the design approach for all the temperature measurements indicated that the cold junction compensators would be located in the vicinity of the related thermocouples. This approach has been changed for several reasons.

Cold junction compensation is now located within the control system interface package. This approach reduces the amount of external wiring to temperature sensors to half. It effects a saving in electronics circuitry and places the compensator in a relatively docile temperature environment. The penalty involved is using thermocouple wire for interconnecting cabling through the structure. Analysis indicates that the accumulated (RSS'd) temperature measurement error is lower for the new approach.

Mounting and temperature environment control for the strain gage pressure sensors is still under consideration. No effect on computer interface design is anticipated.

4.4 CONTROL SYSTEM MONITORING CONCEPTS

The general design philosophy is to provide a highly reliable system, and one in which system degradation can be checked. The system has little or no redundancy; because of this, failure detection is critical, since most failures contribute to dangerous operating conditions.

Fault isolation should be possible at least to the black box level. Due to tight packaging, the removal, and replacement of parts, modules, etc., will be difficult.

Three levels of test monitoring are being considered: one associated with the function of ground support; one in the preflight to prelaunch period; and one after launch through the engine flight tests. These test routines will be executed with the installed sensors providing local environment data to the control system.

Some simulated inputs for checking system degradation will be generated within the computer interface. General tests with a wide range of simulated inputs will be carried out only when the control system components are removed from the engine and coupled to ground checkout equipment.

Components and functional groups will be examined and characterized as to most probable failure modes (e.g., catastrophic failures or degraded operation).

Active failures can be detected by direct means, but care must be taken to ensure that passive failures which may later become critical do not go undetected.

The various detection means will include: (1) limit checks, (2) point calculations based on internally simulated inputs, and, where necessary (3) continuity checks. The digital computer will be used as much as practical in go/no-go evaluations. Provisions are made for inputting the test data via the computer interface. Storage of reference levels and data evaluation will be handled as a software problem, except for one important case which is a failure of the digital computer.

It is assumed that a digital computer failure could immediately create dangerous operating conditions and that the computer itself would be incapable of instituting the engine shutdown sequence. This type of failure requires a simple, highly reliable decision element operating independently of other control system functions.

This outside monitor will turn off power to all control system valve drivers. The electrical power-off conditions for the valves operated by the control system have been defined so that the desired shutdown will occur.

Failure of the outside monitor will have a very high probability of generating system shutdown. Design of the outside monitor should be such that it cannot fail passively and go undetected.

Sensor malfunction (short circuit, open circuit) should be detected or deduced from sensor output measurements. This includes the thermocouples, pressure sensors, and LVDT.

Power supply monitoring is required for fault location. Certain limitations exist in this area since the computer may not be functioning with some power supply failures. These latter failures cannot be sensibly monitored by direct means.

Tradeoffs will be made consistent with the operating characteristics of the control system as a whole. After the design considerations implied have been examined, the scope of the monitoring will be reviewed. In general, all circuit design is proceeding with the above requirements in mind.

4.4.1 Failure Categories

Control system failures can be identified as those potentially structurally dangerous to the engine or the X-15A-2 and those which may induce improper engine operation but do not represent an immediate hazard. "Active failures," (those which generate an unintended action of the driven elements (valves)), will usually fall into the former category. "Passive failures" belong to the category of no immediate hazard and are characterized by a condition which causes no change in operating conditions. A passive failure may, however, become an active failure with a change in operating conditions.

4.4.2 Monitoring Modes and Failure Detection

Active failures can usually be detected immediately, since they represent a departure from predictable operating conditions. End-to-end static accuracy tests can be used to determine component performance degradation. Areas which come directly under this surveillance are sensors, interface electronics, digital computer, actuating valves and aerodynamic and thermal functioning of the engine. Operational monitoring involves two modes. Prelaunch or predrop monitoring will be more comprehensive than the flight test mode. The flight test itself is a relatively short period of time, less than 5 min.; during flight test, digital computer time must be conserved for operational control needs. Consequently, the monitoring at that time is directed to the task of checking for active failures related to loss of control.

Static accuracy tests run during prelaunch are time consuming and would conflict with normal engine operation. Degradation tests of this nature, run continuously until just before launch, justify the launch if no failures are detected. These accuracy tests are essentially end-to-end checks in which known inputs should produce predetermined results for program computations. Since control valves are operating open loop, the test limits are less stringent for these output devices than for the system input signals. A fully operational test of the control valves can only be performed with proper supply pressures available. Consequently, the last check on these devices prior to flight tests will have occurred during ground checkout, before the engine is mounted on the X-15. In flight, prelaunch tests determine that the proper electrical drive has activated the valve torque motors, but these tests do not check the hydro-mechanical section of the valve.

Sensor accuracy, of course, cannot be determined during flight, but comparison of the various sensor inputs provides a means of cross-checking. The digital computer programming includes self-check routines which assess the general health of the computer itself. Outputting a command and reading it at the input provides an end-to-end check on interface electronics. Here again, testing will be more comprehensive during the prelaunch mode than during the flight test.

The electronics interface must, therefore, have the capability to look at its own outputs and to provide the necessary predetermined input signals. Test modes are dictated by stored programs.

4.5 ERROR ANALYSES

Dynamic and component static error studies are continuing in conjunction with the simulation studies and circuit design. The system steady-state error analysis was stopped pending a change in program for the air weight flow and fuel flow computations. This activity should be resumed early in the coming report period.

5.0 ANALYTICAL DESIGN

5.1 DYNAMIC ANALYSIS OF SPIKE SERVOACTUATOR

The last control system development report, Third Interim Technical Data Report, AP-67-3131 discussed the results of a linear analysis of the subject system and also described a nonlinear digital simulation program of the system. No data had been generated at that time.

During the early part of this report period the servoactuators large step and small pertubation characteristics were evaluated using the simulation program; these were reported in detail in AP-68-3250. The system exhibited very stable, overdamped responses at all conditions investigated, and it was concluded that no form of dynamic compensation would be required.

Later, as further mechanical design was completed on the servoactuator, friction loads were revised. Their values became higher and more important, and were defined as varying with actuator velocity, as shown in Figure 5.1-1. The sharp drop in friction loading that occurs when the actuator starts to move is a destabilizing effect, much the same as a negative rate spring might produce. Therefore, it was decided to rerun the simulation with the new friction loads, and the results of that investigation are presented here. The original system was not modified. A 10-gpm servo valve, 3000-psi supply, and 50-psi drain pressure were used.

5.1.1 Load Conditions

A short review of the load conditions is included for the simulation runs discussed below.

The -20°F ambient condition, shown in Figure 5.1-1, is the most severe and was selected for the analysis with the straight-line approximations shown. The total friction force was then defined as the sum of the bearing friction, innerbody seal friction 500 lb, and the actuator locking device 100 lb. The aero forces and spring bellows force used are the same as those used in previous investigations, and are documented in AP-68-3250.

In general, the new friction characteristics had little effect on the performance of the servo.

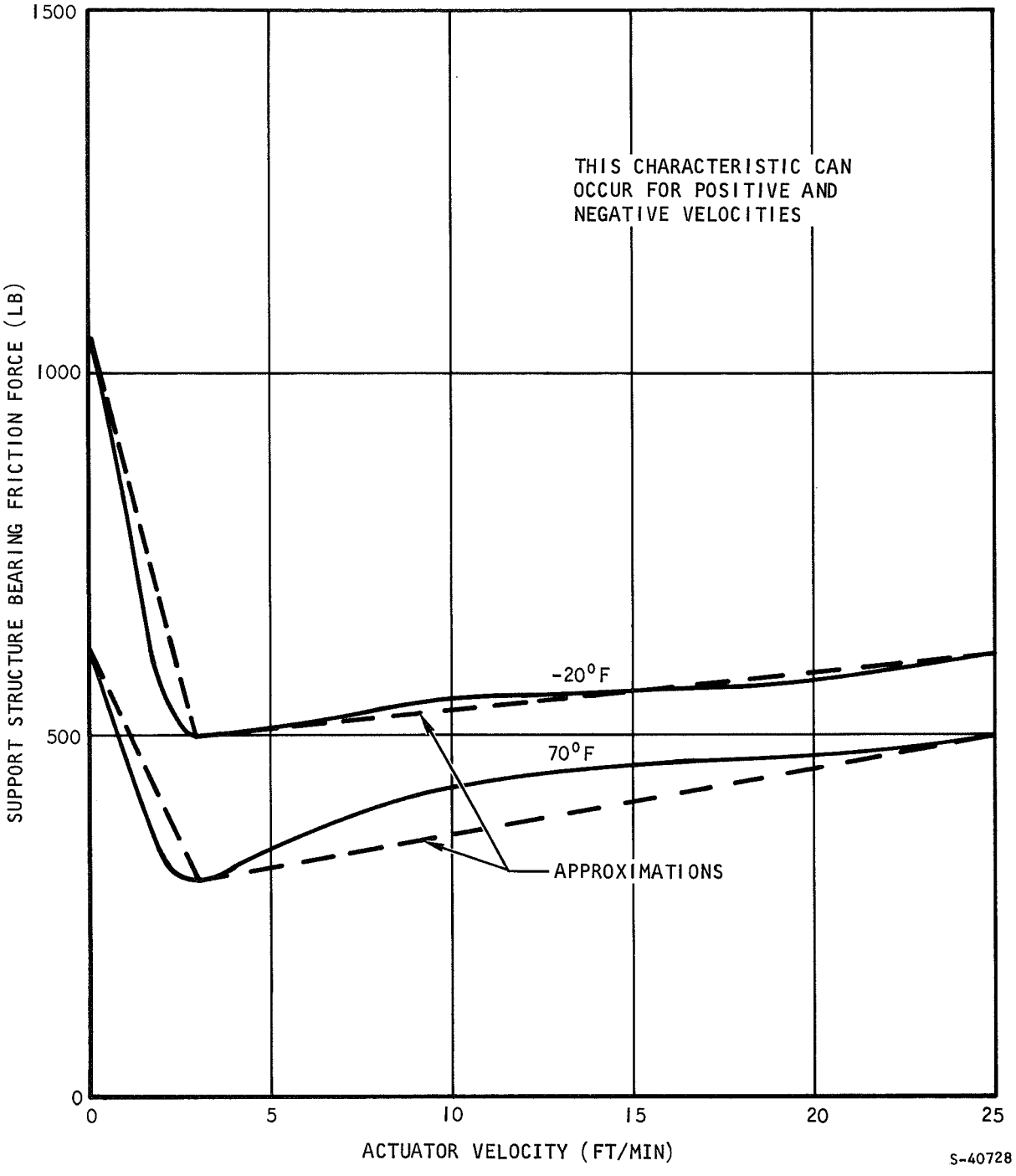

Figure 5.1-1. Support Structure Bearing Friction Force vs Actuator Velocity

5.1.2 Results

5.1.2.1 Small Scale Disturbance

For this run, the actuator is driven to the point of 4-in. retraction, and a steady-state condition is achieved. A small step is then introduced, so that the servovalve is not saturated. Figure 5.1-2 shows that the system is well behaved for a small disturbance. The response is overdamped with no overshoot. Figure 5.1-3 is the response of the system for a small command disturbance that drives the system from 4.4 in. to 4.0 in. Again, the system is well behaved. The net result of the small-scale disturbances is that the destabilized characteristic of the bearing friction force has little or no effect on the servo actuator performance.

5.1.2.2 Large Scale Disturbance

The large-scale analysis is done by introducing step inputs which achieve full retraction-extension strokes. Figure 5.1-4 and 5.1-5 show actuator position and velocity, valve area, and total load force vs time for a retraction-extension sequence. Again, the system is well behaved and overdamped. The total time for a retraction-extension sequence is 1.6 sec.

A comparison of the results for the modified loading with the previous investigations shows very little difference in behavior. For instance, the additional time for a complete retraction-extension sequence is less than 0.1 sec. The maximum retraction velocity is 0.2 in./sec slower; the maximum extension velocity is also 0.2 in./sec slower. The maximum and minimum load forces are 1000 lb different in each direction than those of the previous analysis.

5.1.3 Effect of Supply Pressure Variation

The effects of supply pressure transients were also considered. These effects might be caused by dynamics of the nitrogen pressure regulator in combination with line losses and lags. The transient used for the retraction stroke is shown in Figure 5.1-6. In this direction the aero loads aid the motion and the supply pressure is reduced almost 500 psi by the initial rapid actuator velocity. Near the end of the transient, supply pressure peaks at some 2200 psi when the control valve is closed. The hydraulic supply system was not simulated; instead, supply pressure transients (Figure 5.1-6) were programmed into the simulation. There was little difference in the centerbody servo-actuator performance as a result of supply pressure transients. Typical results are shown in Figures 5.1-7 and 5.1-8. A small lag (maximum of 0.020 in.) in actuator position caused by the drop in supply pressure is shown in Figure 5.1-7. However, the actuator tends to catch up to the constant supply case near the end of the transient when the pressure peaks (Figure 5.1-8). It is if supply pressure transients are no worse than shown in Figure 5.1-6. There will be very little effect on the servo actuator performance.

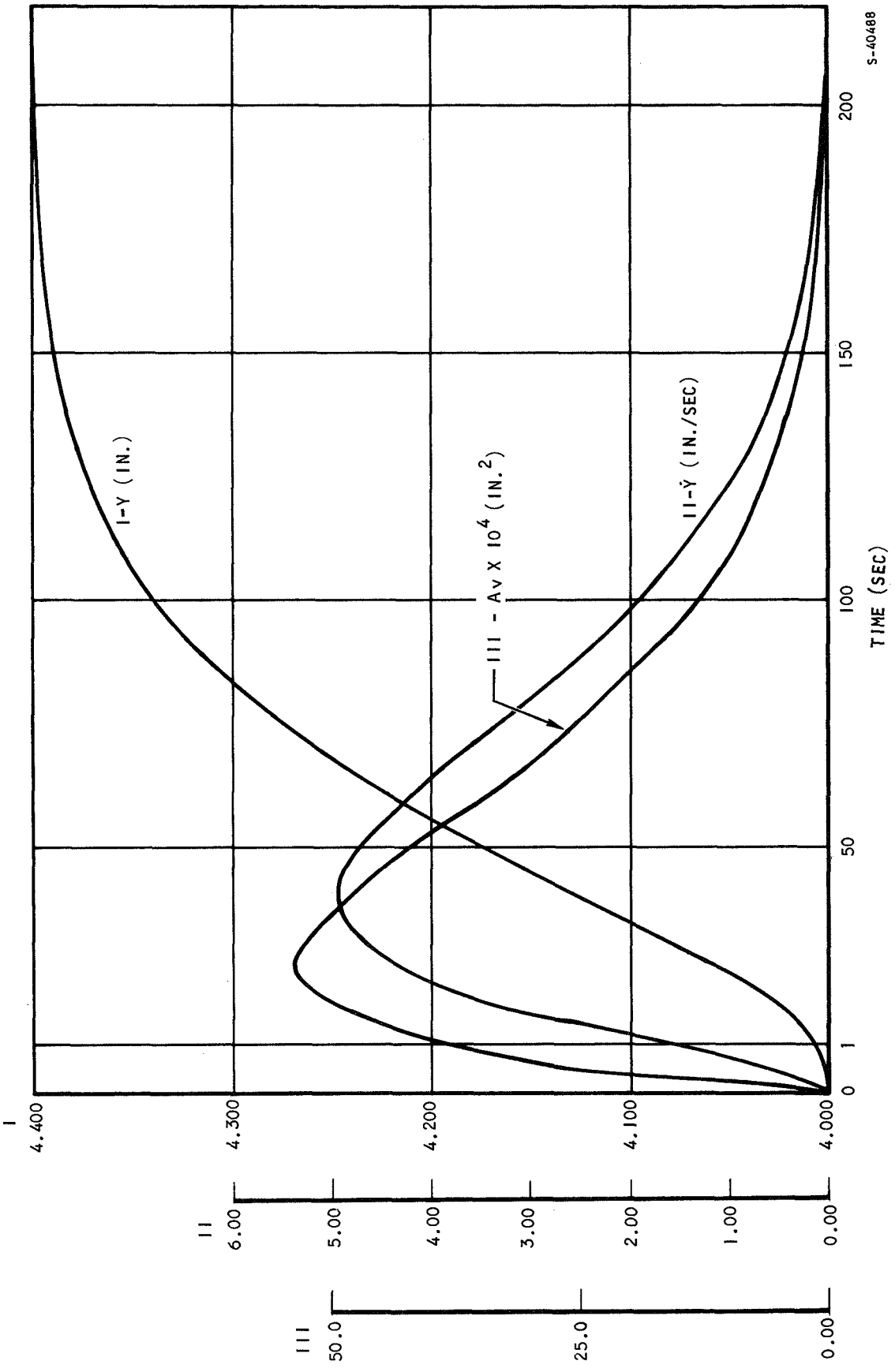

Figure.5.1-2. Small Step from 4.0 to 4.4 in.

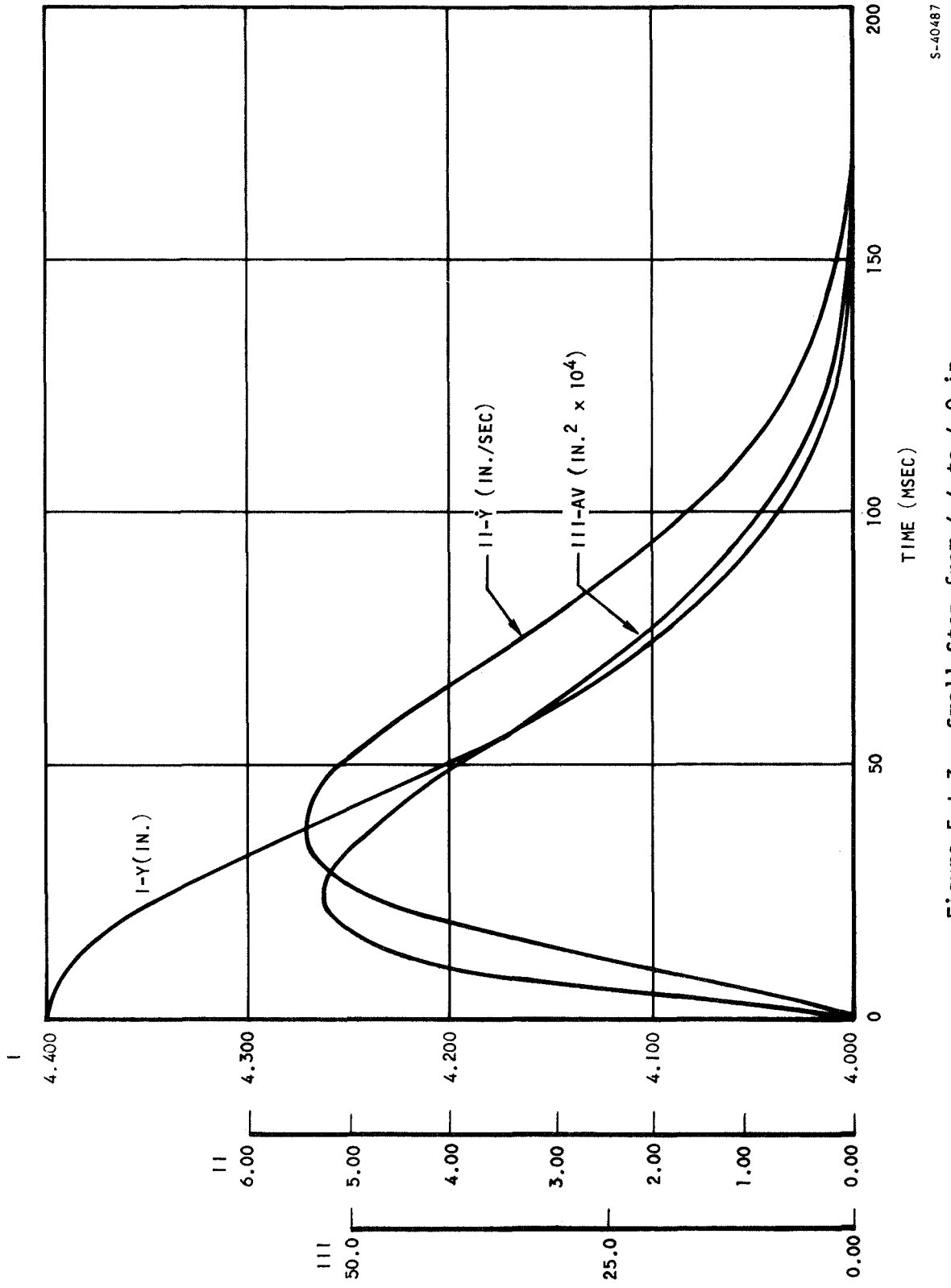

Figure 5.1-3. Small Step from 4.4 to 4.0 in.

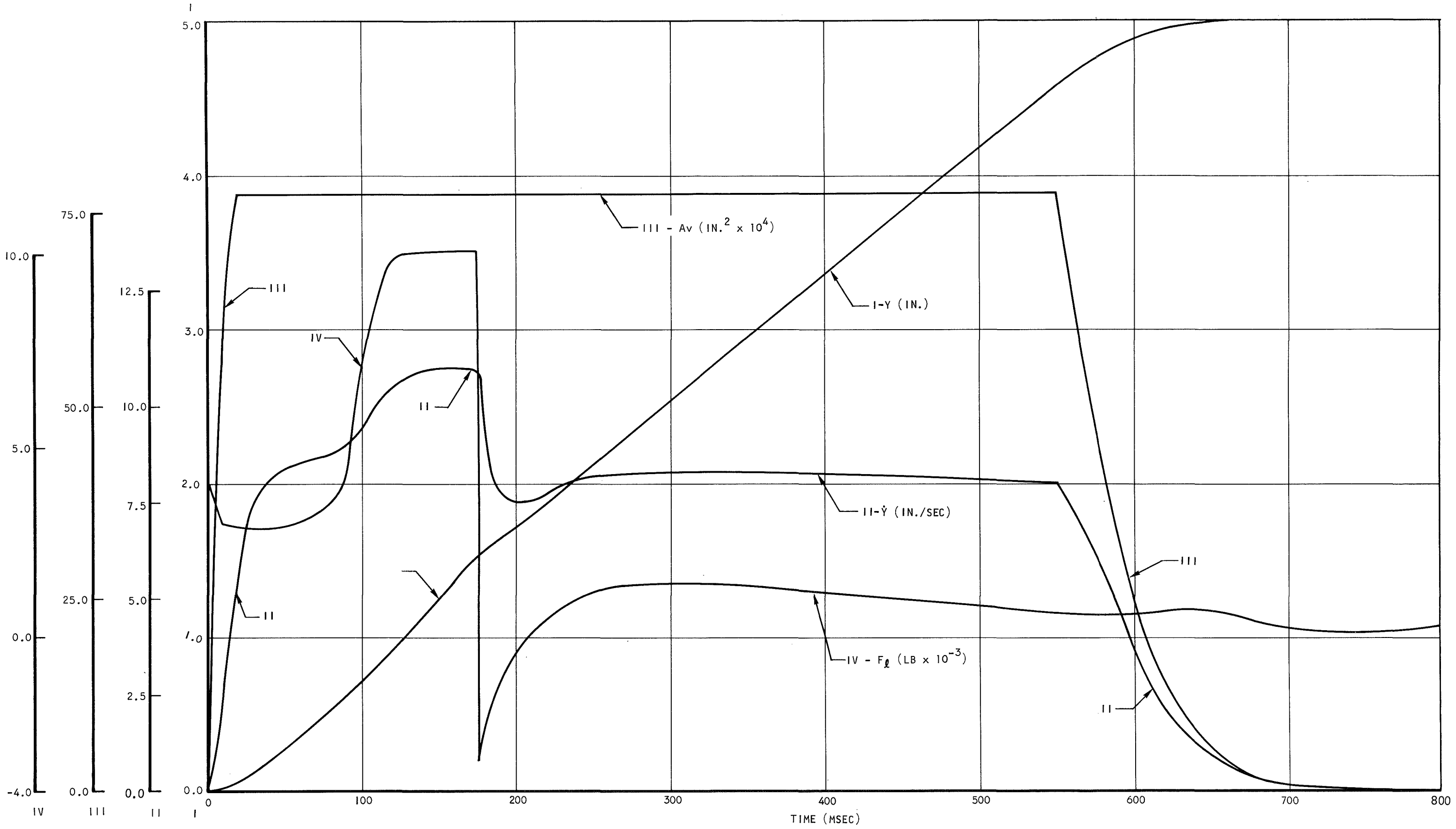

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Figure 5.1-4. Full Retraction Sequence with Modified Friction Loading

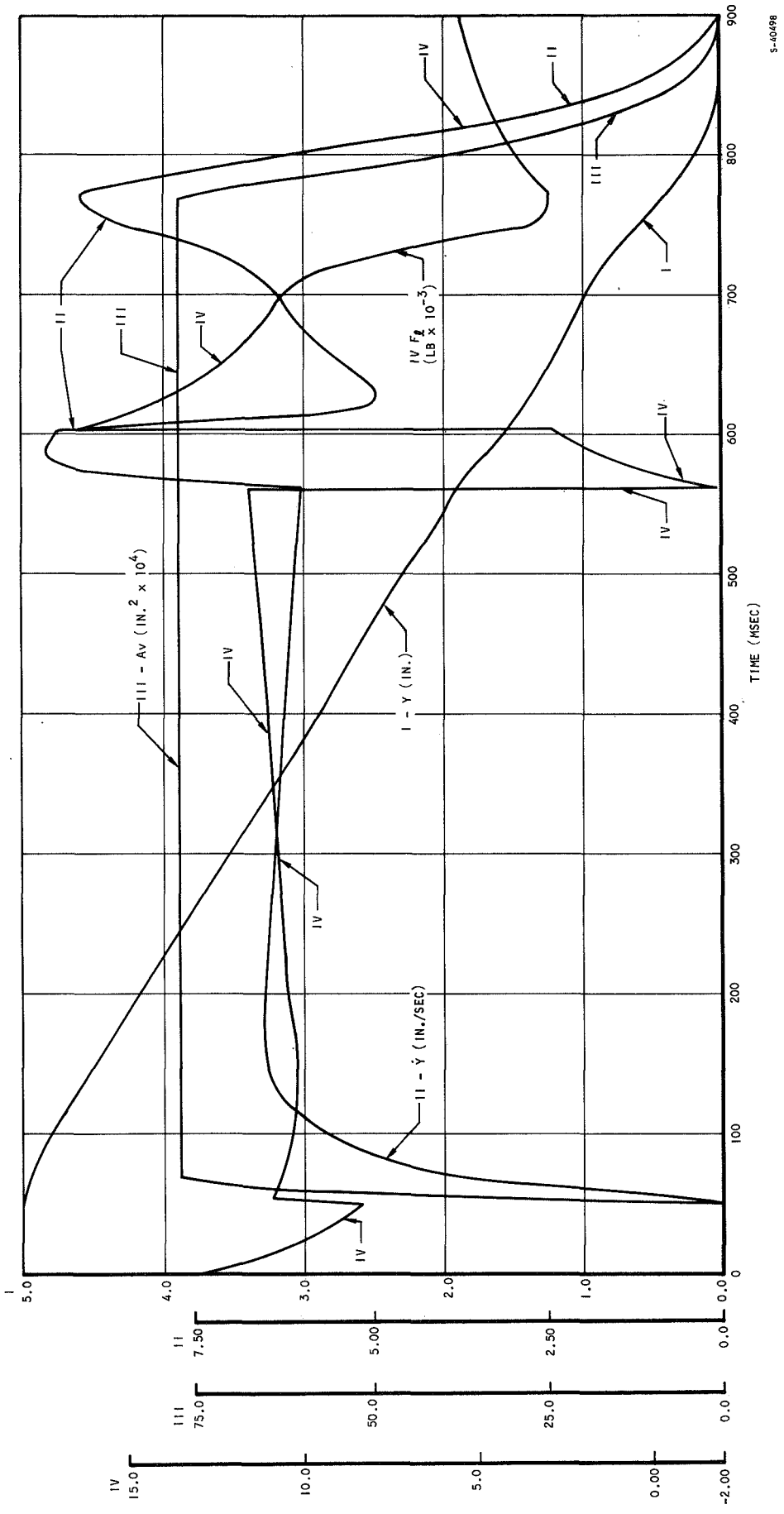

Figure 5.1-5. Full Extension Sequence with Modified Friction Loading

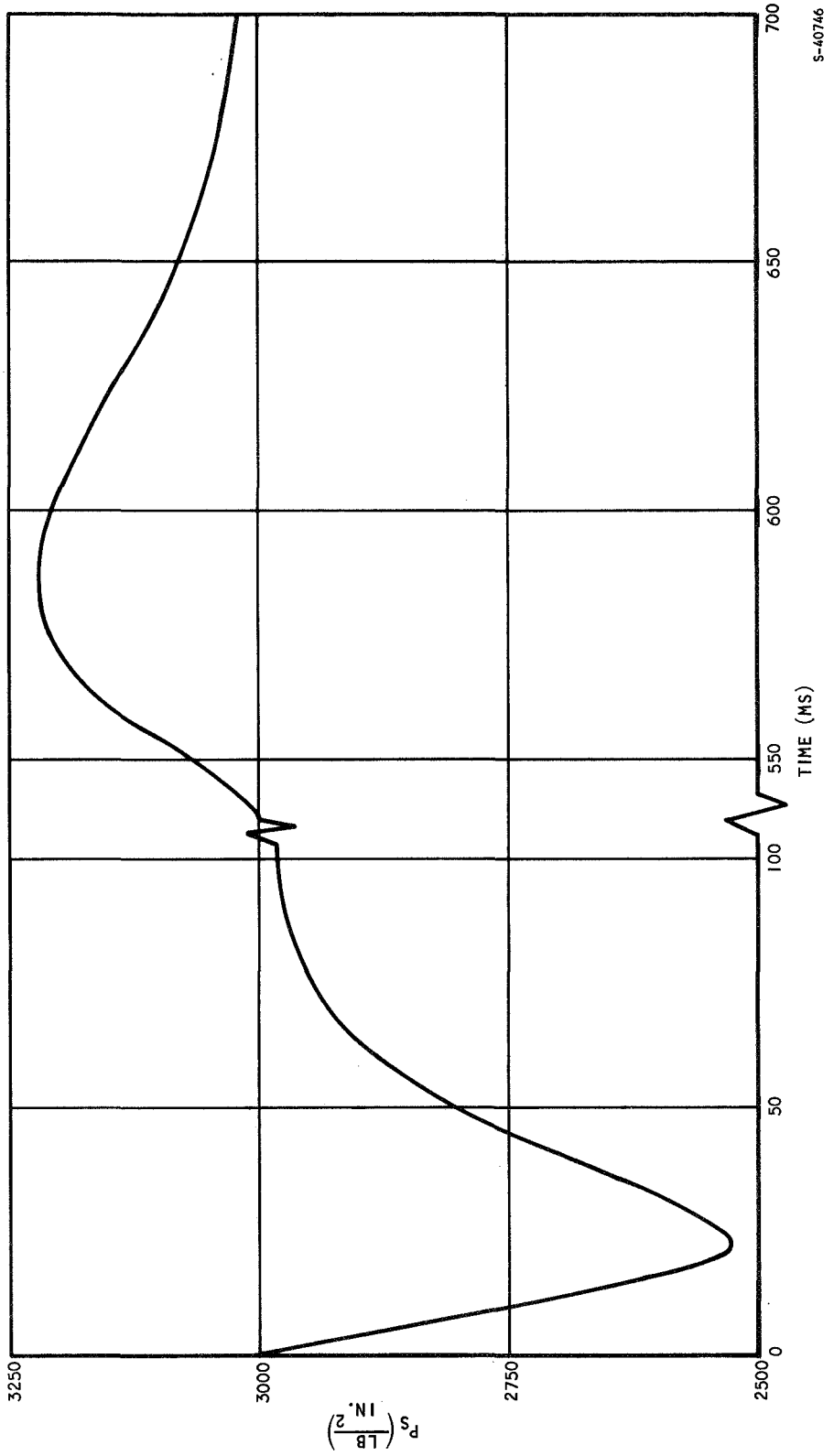

Figure 5.1-6. Supply Pressure Transient for Retraction Stroke

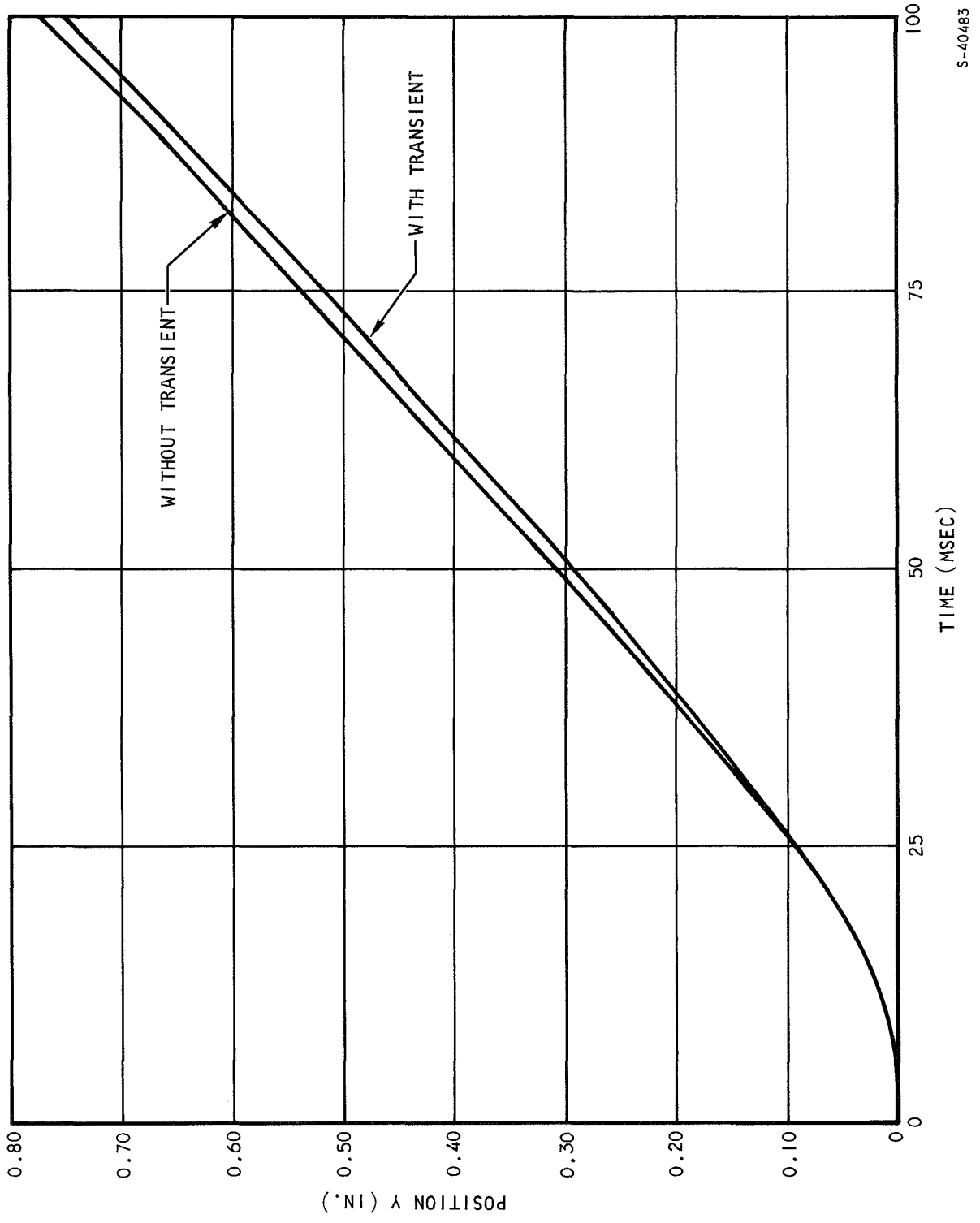

Figure 5.1-7. Retraction Sequence

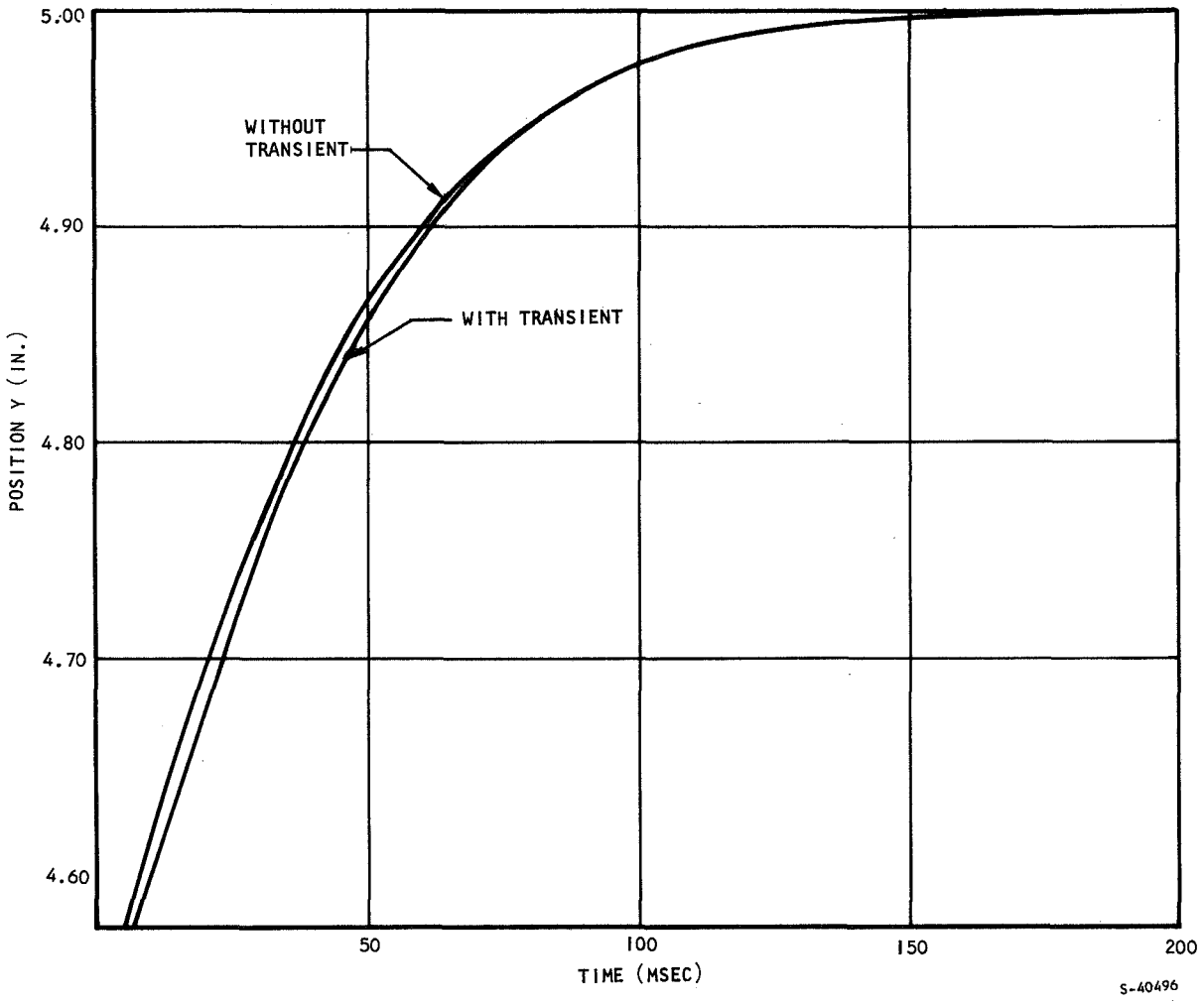

Figure 5.1-8. Retraction Sequence

5.1.4 Summary

The conclusions reached for the previous analysis of the centerbody actuator can again be stated for this analysis with the modified friction loading:

(a) The control characteristics of the proposed hydraulic centerbody servo actuator are good. The system has an overdamped response for both retraction and extention sequences.

(b) Abrupt changes of the load forces which occur with inlet start and unstart sequences have little effect on the performance of the system.

(c) The servo actuator is also well behaved for small linear transients.

(d) Neglecting all leakages, a full retraction-extension sequence requires 50 $in.^3$ of hydraulic fluid.

(e) Total time for a complete cycle is 1.6 sec.

Unless major changes occur in system mechanization, or new loading definitions are encountered, the hydraulic centerbody servo actuator nonlinear analysis is complete. Further investigations cannot be justified at this time. Minor discrepancies will undoubtedly appear when the model is completed and tested, and investigations on the test stand should be conducted to verify these computer runs.

5.2 MATHEMATICAL MODEL STUDIES

Analog simulation of the cooling system has been checked out, and has undergone three phases of testing: (1) static tests, in which the simulator was used to produce steady-state pressures and flows for varying valve areas and injector flows; (2) open-loop frequency response tests, in which the bandwidth of the response of various flows to changing valve area was measured; and (3) closed-loop tests of the innerbody temperature control, which were used to provide initial design of compensation and to establish preliminary design data for development of the breadboard control.

Many refinements have been introduced into the simulator to reduce noise, decrease the number of components used, etc. The simulator has been completely repatched; the most recent set of wiring details is presented in Appendix A.

Because the original simulator models (the individual heat exchangers) could not match the predicted transient coolant response, an independent study of the simulation of the heat exchangers has been undertaken. A new model of the innerbody heat exchanger, developed from this study, was used in the closed-loop tests.

5.2.1 Report on Analog Computer Simulation for the HRE Heat Exchanger

The problem is analog computer simulation of a regenerative cooling system for the hypersonic research engine. The engine fuel (hydrogen) is circulated in the body to achieve the desired cooling. Depending on flight conditions, the desired mass flow rate (lb/sec) is passed through the body by using an active temperature control system.

A typical section of the engine skin and its dimensions are shown in Figure 5.2-1.

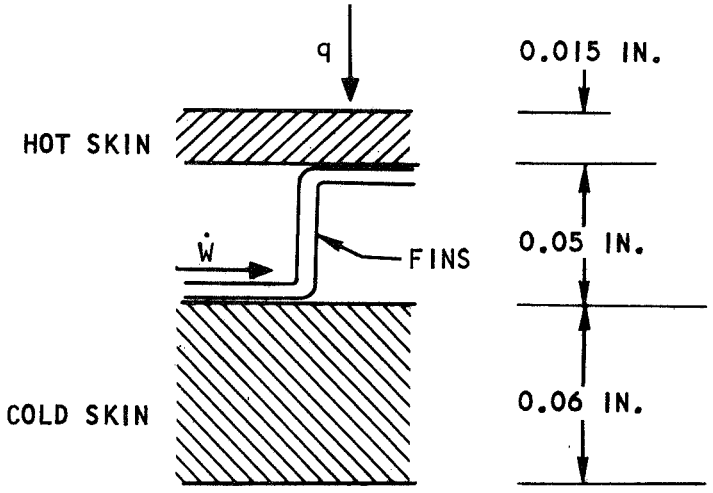

Figure 5.2-1. Cross-Section of the HRE Heat Exchanger

A detailed digital computer simulation has been performed for the system and the results of this simulation are shown in Figures 5.2-2 through 5.2-9. An analog simulation is needed to match the results obtained from the dig tal analysis.

In digital computer simulation, the heat exchanger (50-in. long) was divided into three sections; energy balance equations were used to calculate the different temperatures. This procedure was used until the inlet coolant temperature was obtained. In Figures 5.2-10 and 5.2-11: T(3, 17, 31, 20, 22, 23, 24, 26, 28) are metal node temperatures and T(71, 72, 73, and 74) are the coolant temperatures. T71 is the inlet coolant temperature and it is held at a constant -360°F. Some of the heat given to the hot skin is stored in the wall and the rest is passed on to the coolant. It is assumed that there is no axial heat transfer in the metal. (Since the effective heat transfer coefficient $\frac{kA}{x}$ is very small the heat transfer which occurs between, say, T(3) and T(17) can be neglected.) The temperature gradient in the wall is shown in Figures 5.2-8 and 5.2-9.

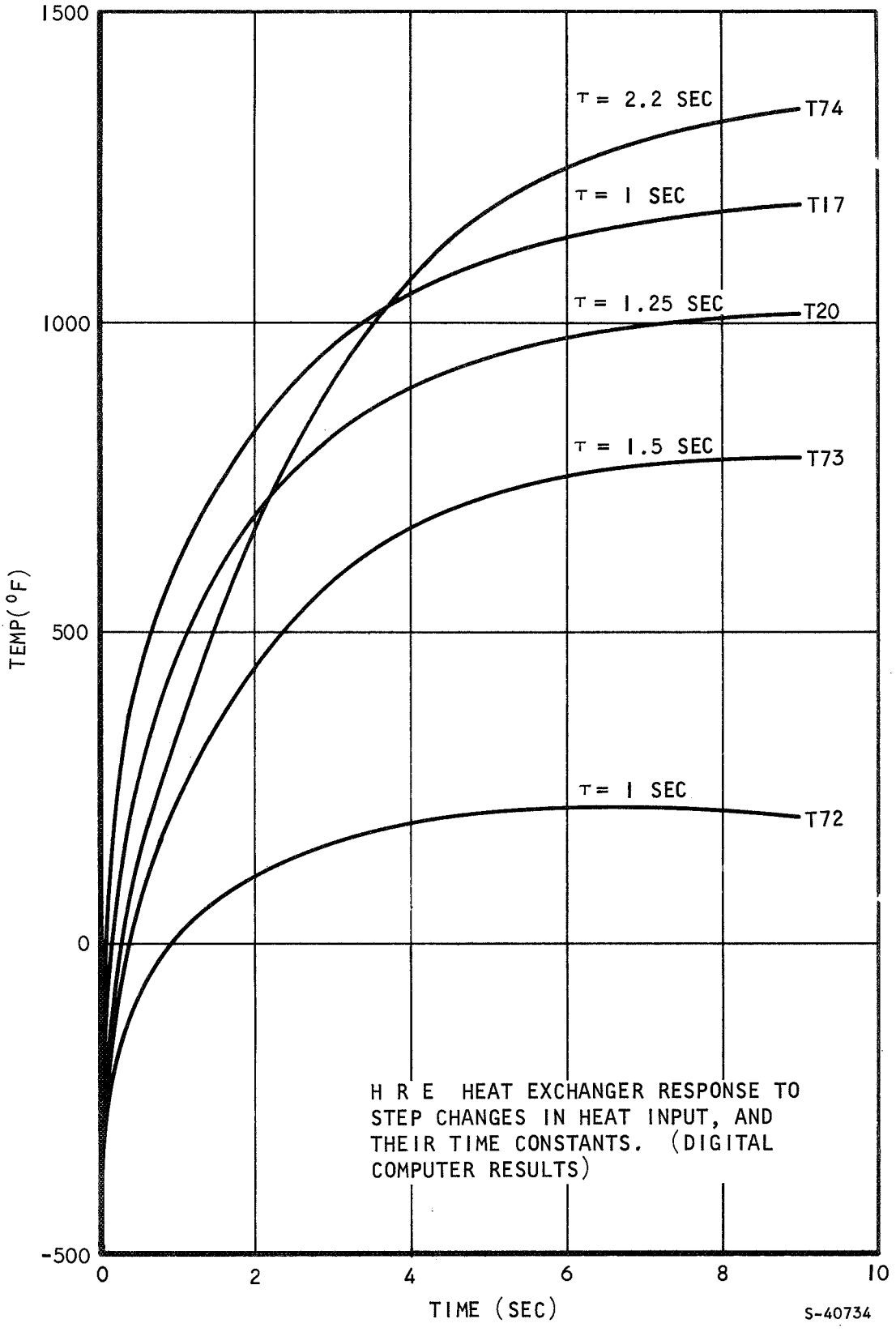

Figure 5.2-2. Case IA

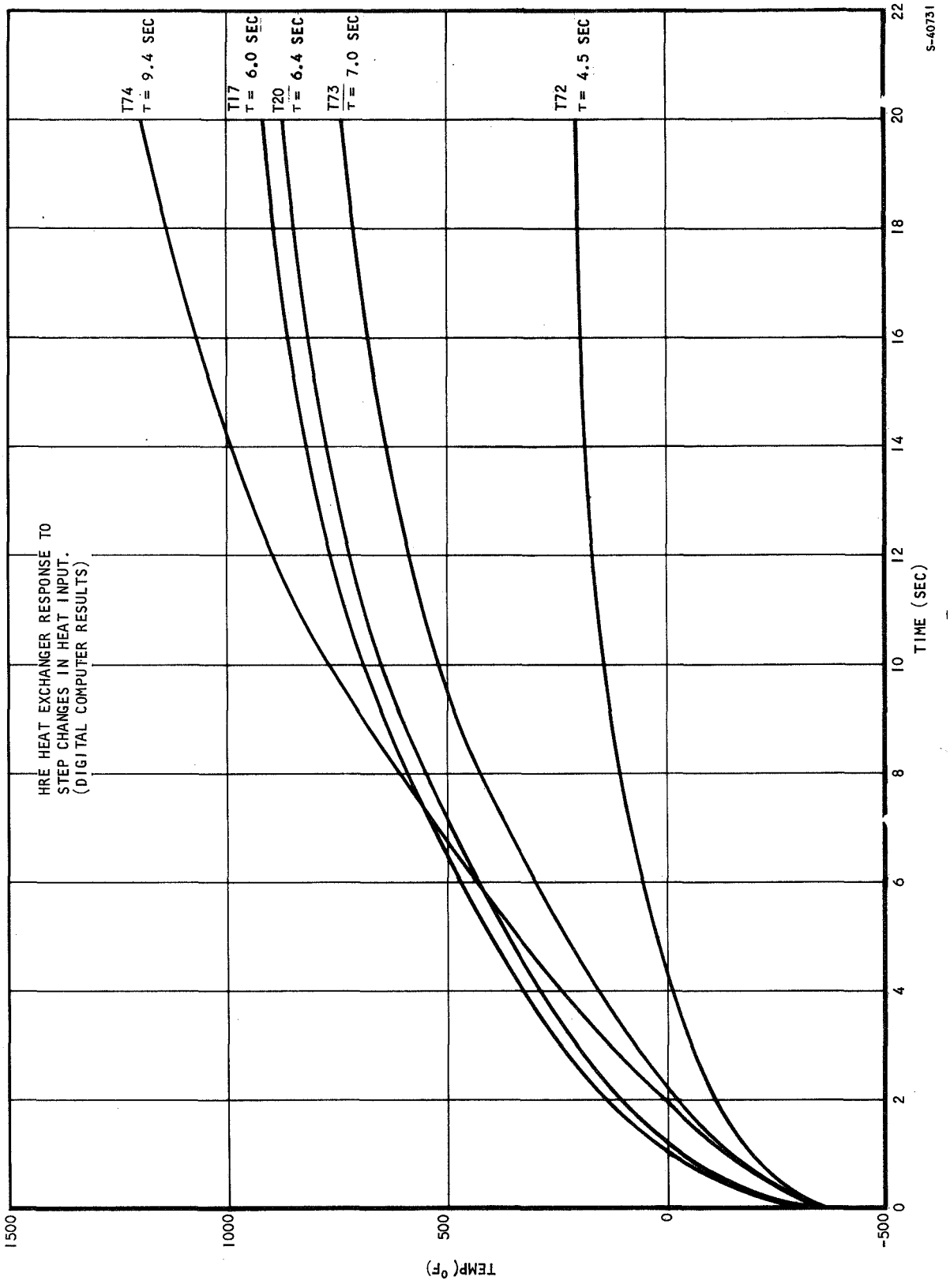

Figure 5.2-3. Case IB

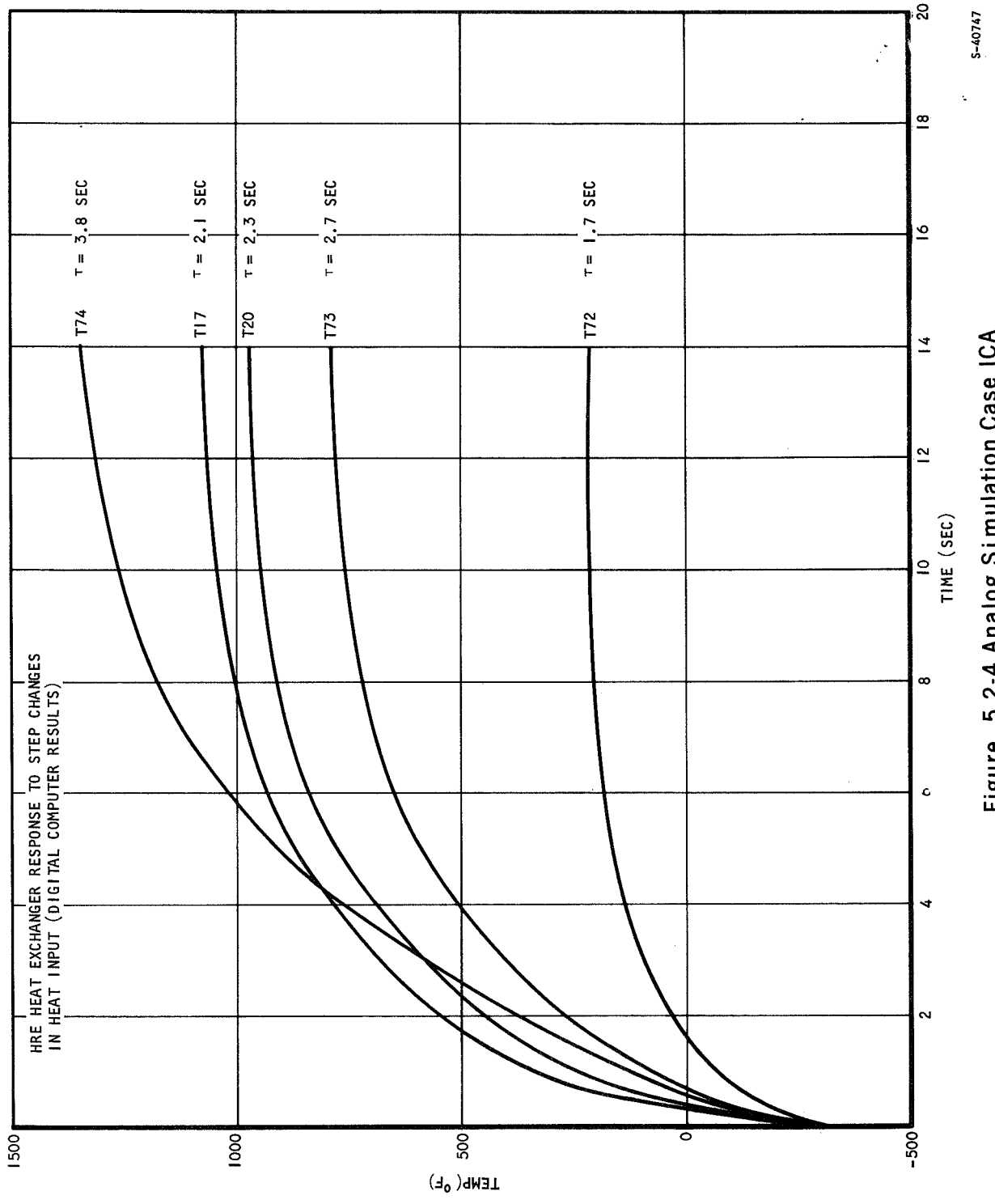

Figure 5.2-4 Analog Simulation Case ICA

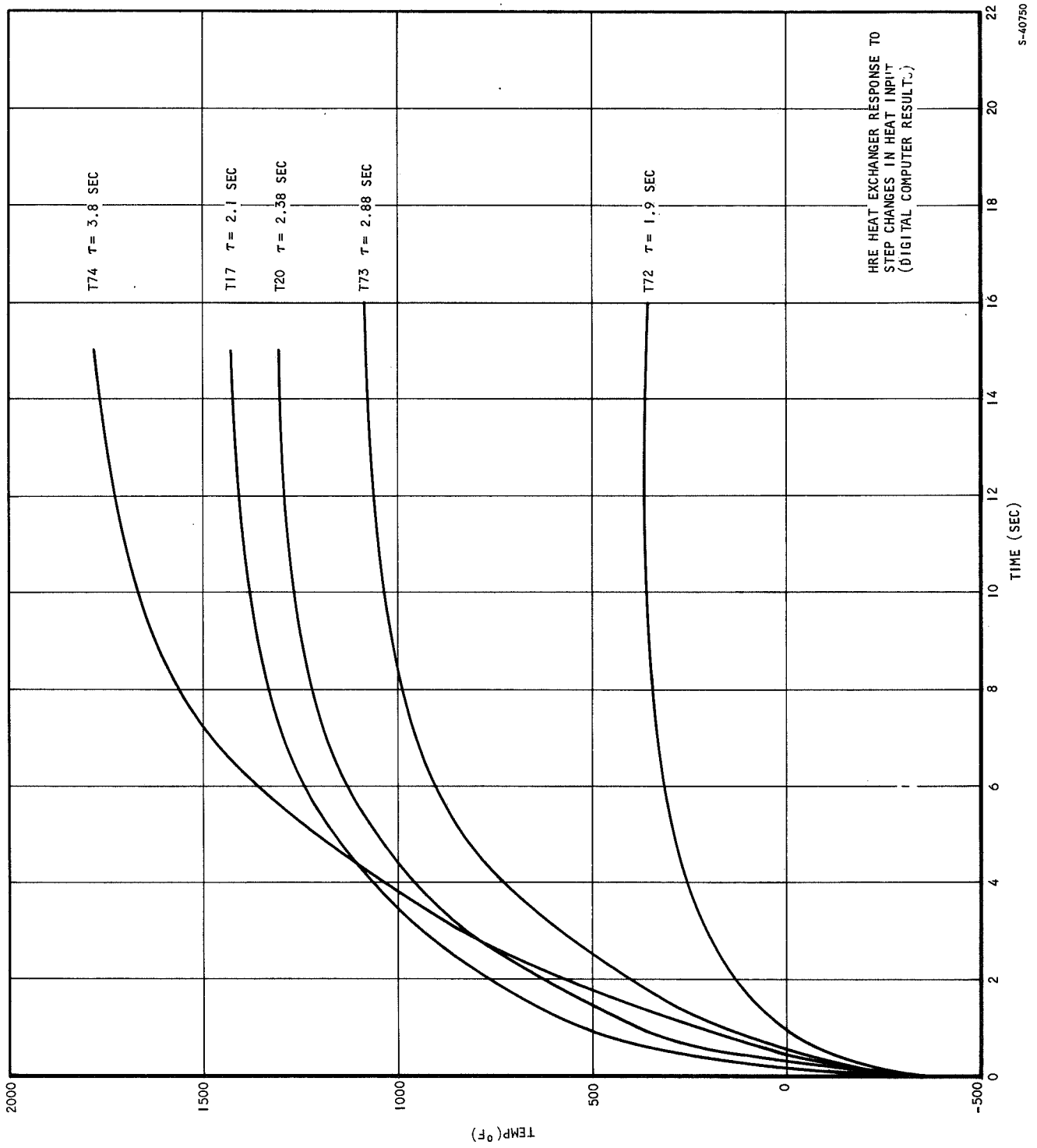

Figure 5.2-5. Case ICB

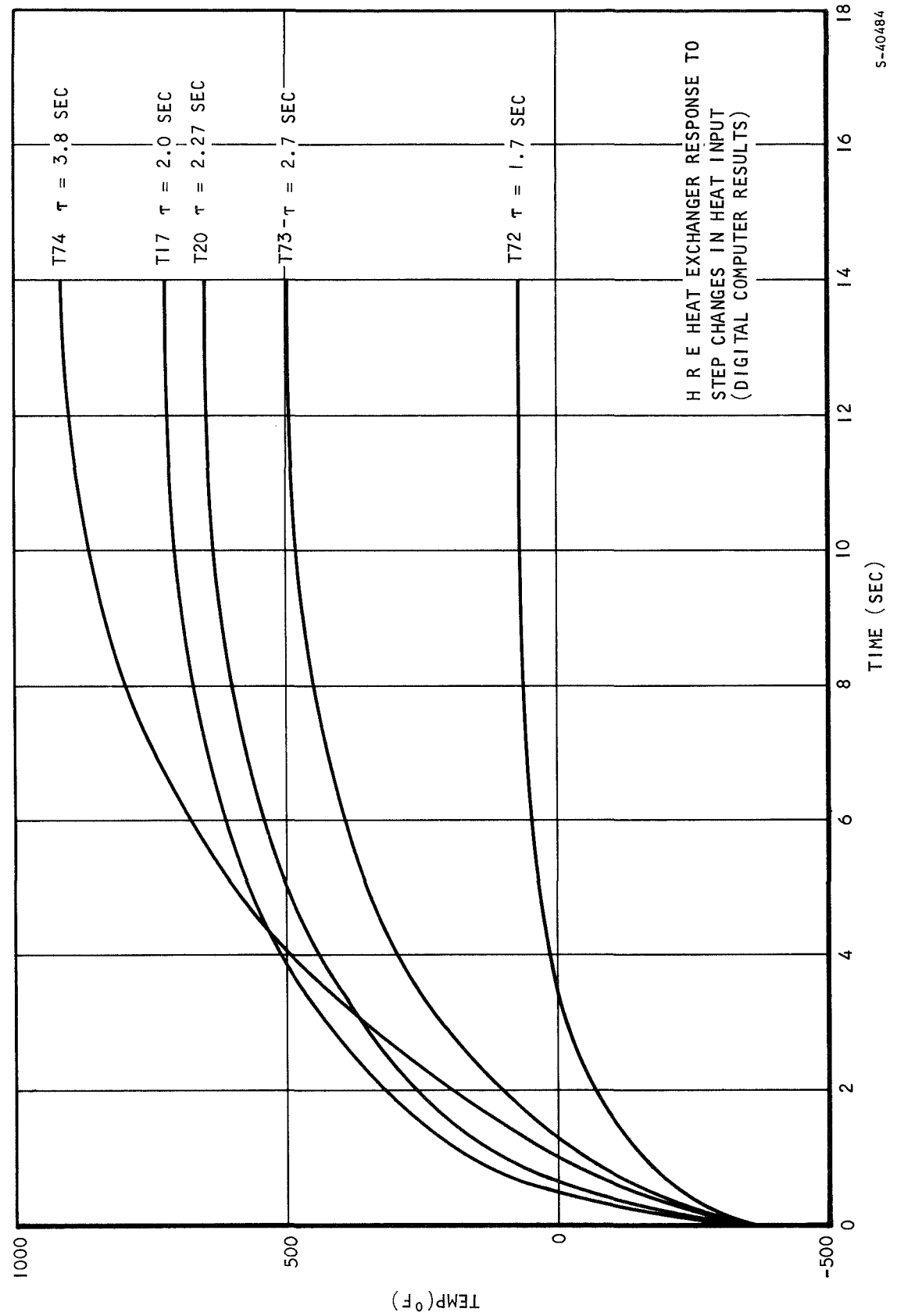

Figure 5.2-6. Case ICC

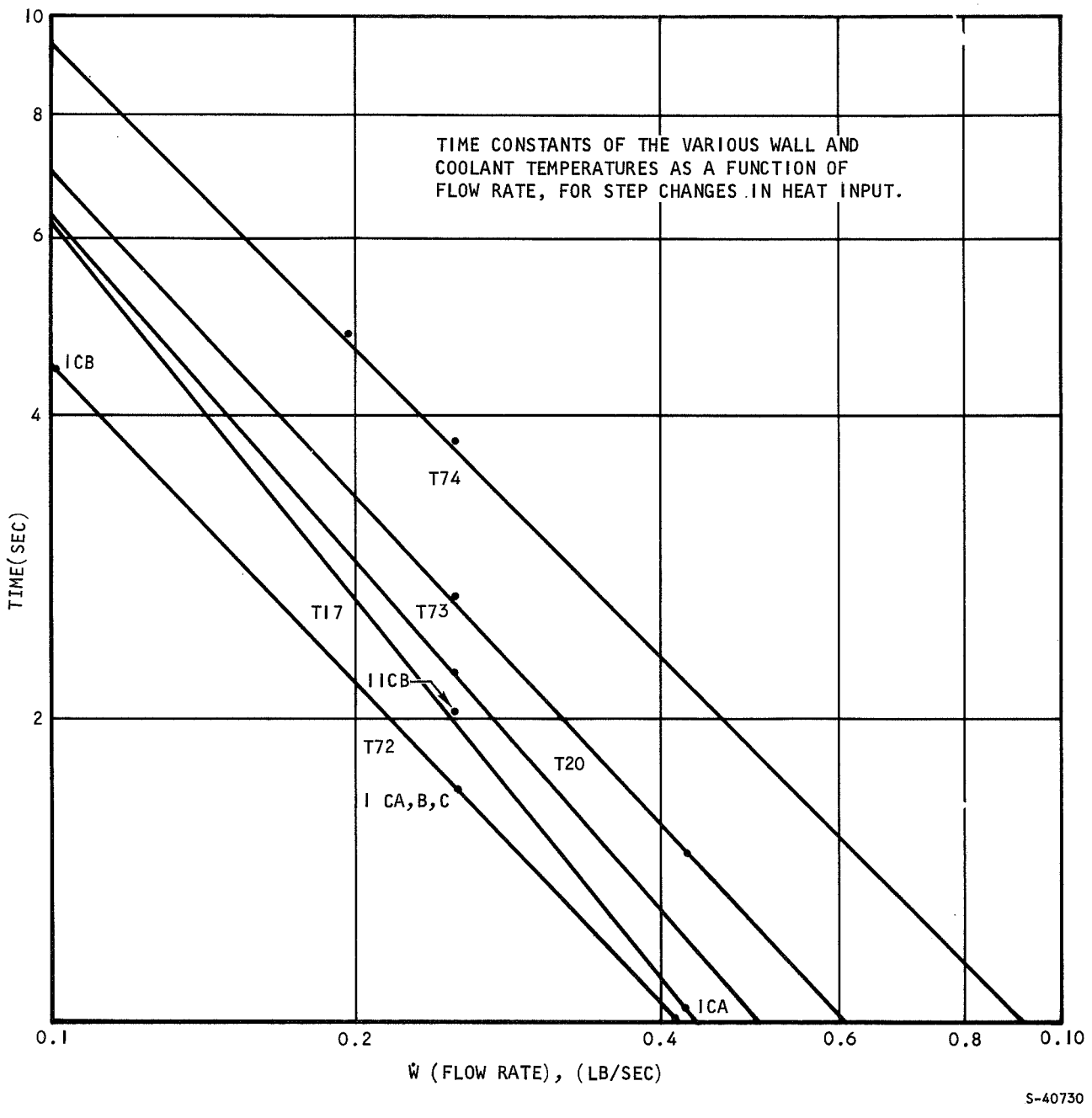

Figure 5.2-7. Time Constant vs Flow

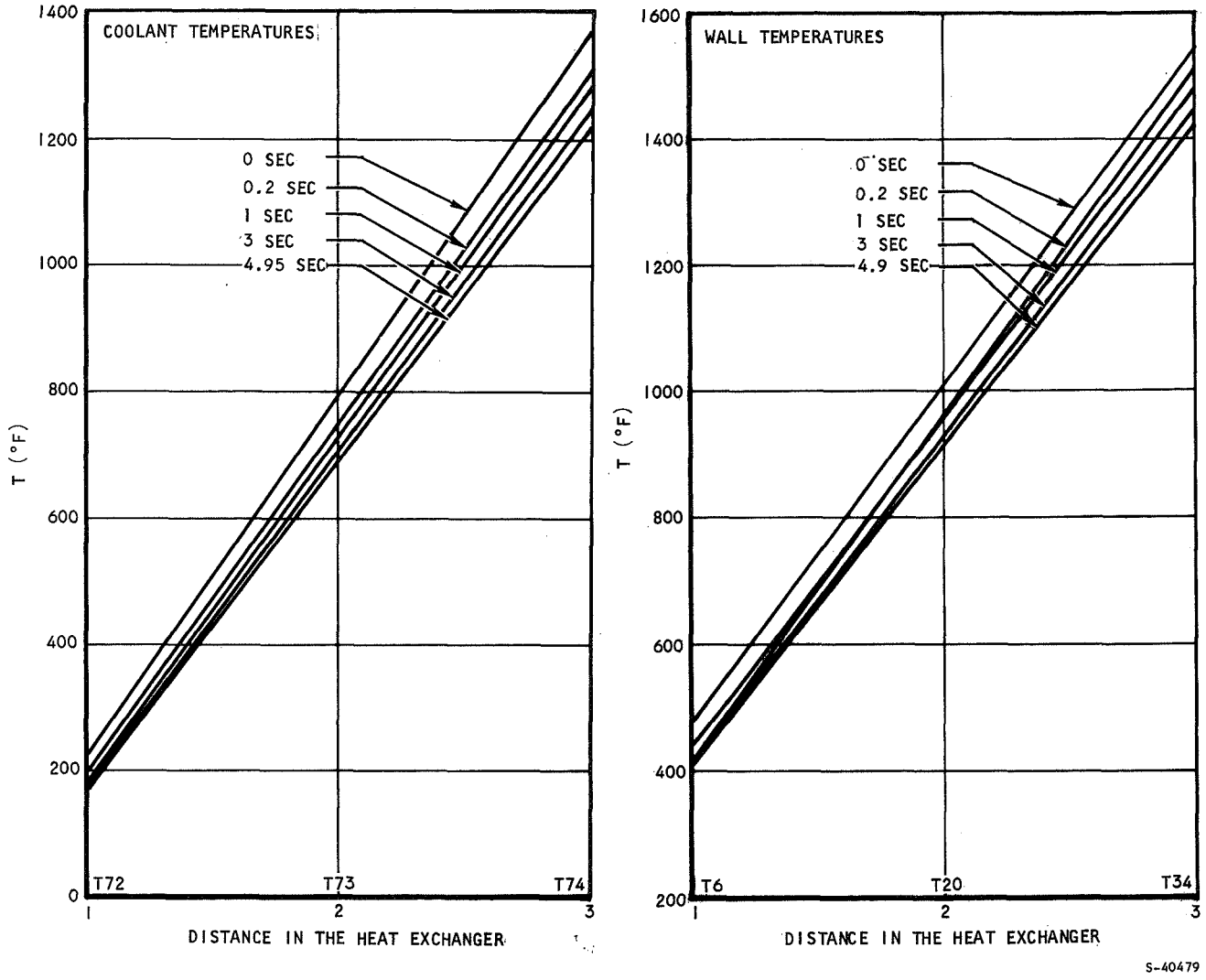

Figure 5.2-8. Temperature Profiles

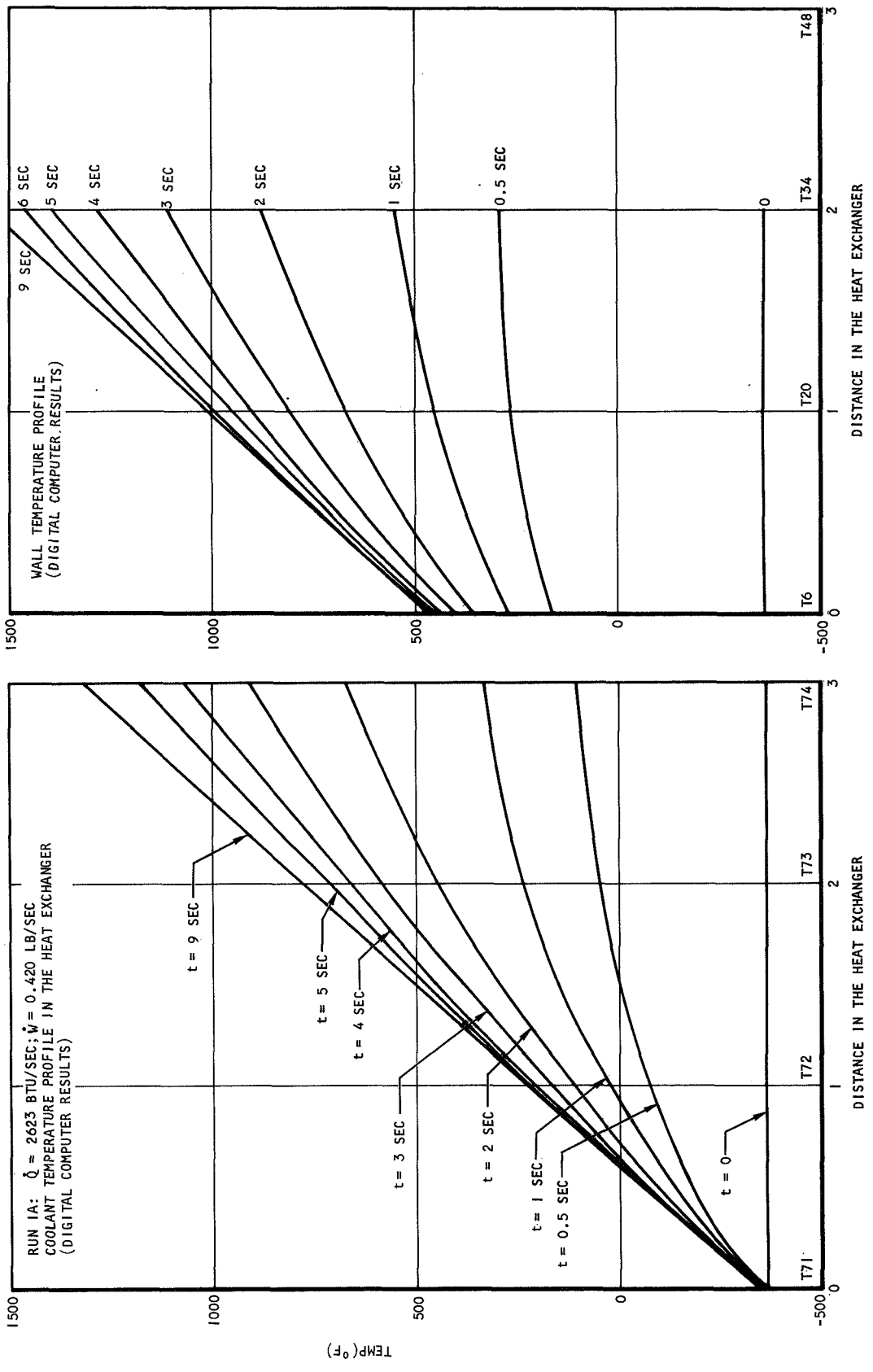

Figure 5.2-9. Temperature Profiles: Case IA

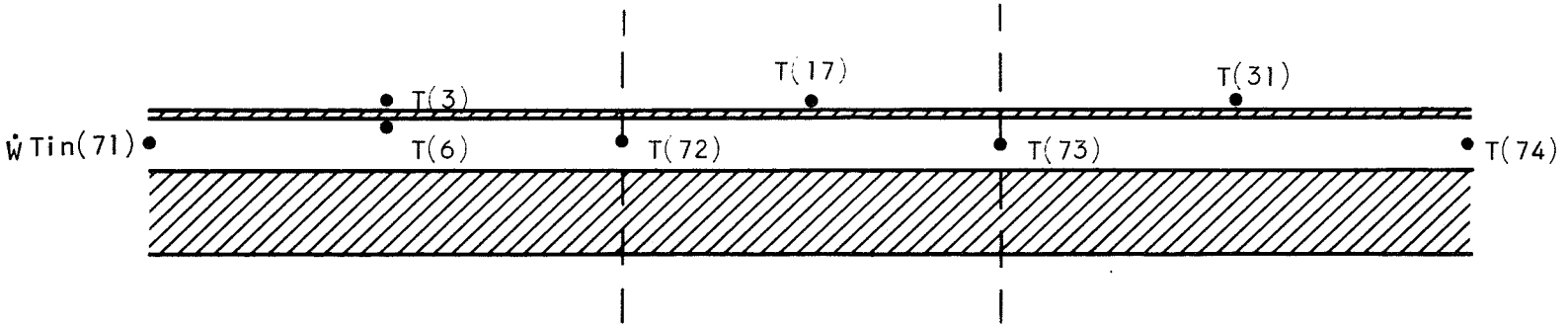

Figure 5.2-10. Digital Computer Representation of Heat Exchanger

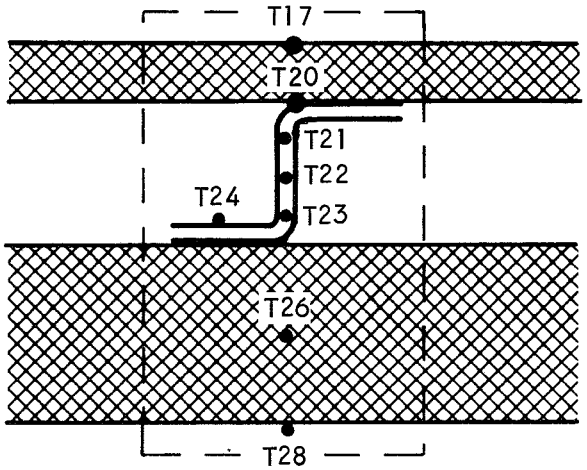

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Figure 5.2-11. Digital Computer Representation of Heat Exchanger

In calculations concerning the heat transfer between the metal and the coolant, an average coolant temperature is used. For example, for the first node (section) a coolant temperature used is

$$\frac{T(71) + T(72)}{2}$$

The above model, and the results obtained using it, will be frequently referred to in the following sections. To avoid repetition, no equations are given here. However, the equations that will be used for the analog simulation will be similar to the digital ones.

5.2.1.1 Analysis of the Analog Computer Simulation

Given the above configuration and the heat transfer equations, an analog computer model could be obtained, but the number of amplifiers required to do this would make the simulation impractical. Hence, a model using a smaller number of amplifiers was sought.

Since the digital computer results were available, some observations that would simplify the model could be made. The first was the fact that the temperature gradient across the cold skin was negligible and, therefore, the heat transfer between the coolant and the cold skin could be ignored. Although this observation was based on the results obtained, a closer look at the system configuration would have yielded the same results; since the cold skin mass is much larger than the hot skin, the temperature gradient will be very small and the heat transfer across the wall will be negligible.

The next simplification was to use one section, rather than three used in the digital simulation. This simplification could be justified if the response of the outlet temperature was first order. Then the analog simulation would reduce down to a system with a first-order time constant. From the digital computer results it was observed that the above assumption concerning the behavior of the outlet coolant temperature was indeed true for the step increases in heat input.

By keeping the above assumptions, the following simplified version of the heat exchanger is possible.

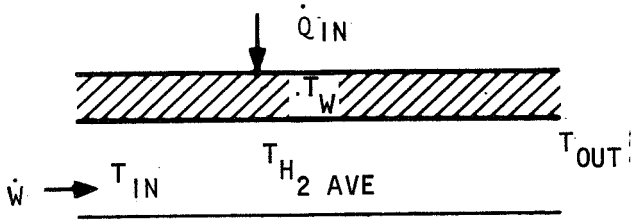

Figure 5.2-12. Analog Computer Representation of Heat Exchanger

Using the heat transfer formulas, the following equations can be derived which govern the heat exchanger.

$$\dot{Q}_{IN} - \dot{Q}_{H_2} = MwCpw \frac{dTw}{dT} \tag{5-1}$$

$$\dot{Q}_{H_2} = W\ Cp\ (T_{out} - T_{in}) \tag{5-2}$$

$$\dot{Q}_{H_2} = A_o\ \eta_T h_c \left(\frac{A_t}{A_o}\right)\ (Tw - T_{H_2\ ave}) \tag{5-3}$$

The first equation simply states that the difference between heat in and heat out of the wall is stored in the wall. This stored heat is $MwCpw \frac{dTw}{dT}$, where Mw and Cpw are the mass and the heat capacity of the wall and $\frac{dTw}{dT}$ is the rate of change of the wall temperature.

Equation (5-2) states that the enthalpy increase of the coolant is equal to the heat taken by the coolant, and equation (5-3) yields the heat which is given off to the coolant by the wall.

In equation (5-3), A_o is the area of the heat exchanger, A_t is the total area (including the fin area), and η_T is the efficiency of the fin. The term $\eta_T h_c \left(\frac{A_t}{A_o}\right)$ is obtained empirically and is given below.

$$\eta_T h_c \frac{A_t}{A_o} = 0.776 \left(\frac{\dot{W}}{0.42}\right)^{0.8} \tag{5-4}$$

The other constants occurring in equations (5-1) through (5-3) are:

A_o = 1800 in.^{2}

Cp = 3.6 Btu/lb$_m$ ^oR

Cp_{wall} = 0.10 Btu/lb$_m$ ^oR

If one assumes that $T_{ave} = \frac{T_{out} + T_{in}}{2}$, equation (5-3) can be replaced by equation (5-5).

$$Q_{H_2} = A_o\ \eta_T h_c \left(\frac{A_t}{A_o}\right) \left(Tw - \frac{T_{out} + T_{in}}{2}\right) \tag{5-5}$$

In the above equations there are three unknowns ($\dot{Q}_{H_2}$, Tw, T_{out}) and three equations (5-1), (5-2), and (5-5). At this point, one more simplification was introduced. If there is no heat loss to the ambient surroundings, equation (5-2) is equal to (5-5).

$$\dot{W}C_p\,(T_{out} - T_{in}) = A_o\,\eta_T h_c \left(\frac{A_t}{A_o}\right)\left(Tw - \frac{T_{out} + T_{in}}{2}\right) \qquad (5\text{-}6)$$

or

$$\dot{W}C_p\,(T_{out} - T_{in}) = A_o\,0.776\left(\frac{\dot{W}}{0.42}\right)^{0.8}\left(Tw - \frac{T_{out} + T_{in}}{2}\right) \qquad (5\text{-}7)$$

By defining a constant $K = \dfrac{A_o\,(0.776)}{(Cp)(0.42)^{0.8}}$ one can further simplify equation (5-7) to obtain equation (5-8).

$$\dot{W}\,(T_{out} - T_{in}) = K\,\dot{W}^{0.8}\left(Tw - \frac{T_{out} + T_{in}}{2}\right) \qquad (5\text{-}8)$$

Now, T_{out} can be obtained from equation (5-8)

$$2\dot{W}\,T_{out} - 2\dot{W}\,T_{in} = 2K\,\dot{W}^{0.8}\,Tw - K\,\dot{W}^{0.8}\,T_{out} - K\,\dot{W}^{0.8}\,T_{in}$$

$$T_{out}\,(2\dot{W} + K\,\dot{W}^{0.8}) = T_{in}\,(2\dot{W} - K\,\dot{W}^{0.8}) + 2K\,\dot{W}^{0.8}\,Tw$$

$$T_{out} = \frac{(2\dot{W} - K\,\dot{W}^{0.8})}{2\dot{W} + K\,\dot{W}^{0.8}}\,T_{in} + \frac{2K\,\dot{W}}{2\dot{W} + K\,\dot{W}^{0.8}}\,Tw \qquad (5\text{-}9)$$

One can call (for W = constant) the coefficients in front of T_{in} and Tw, C_1 and C_2 respectively. $(C_1 + C_2 = 1)$

$$T_{out} = C_1\,T_{in} + C_2\,Tw \qquad (5\text{-}10)$$

A table which gives C_1 and C_2 for different flow is given in a later section.

For reference, the original equations, computer equations, and scaling factors are shown

$$\dot{Q}_{IN} = \dot{Q}_{H_2} = Mw\,Cpw\,\frac{dTw}{dT} \qquad (5\text{-}11)$$

$$\dot{Q}_{H_2} = \dot{W}\, C_p\, (T_{out} - T_{in}) \tag{5-12}$$

$$T_{out} = C_1\, T_{in} + C_2\, Tw \tag{5-13}$$

Variable	Estimated Maximum	Computer Variable
$\dot{Q}_{IN}$	5000	$\dot{Q}/5000$
$\dot{Q}_{H_2}$	5000	$\dot{Q}_{H_2}/5000$
T_{in}	2000	$T_{in}/2000$
T_{out}	5000	$T_{out}/5000$
$\dot{W}$	1	$\dot{W}/1$

Computer Equations

$$5000\, \frac{\dot{Q}_{IN}}{5000} - \frac{\dot{Q}_{H_2}}{5000}\; 5000 = MwCpw\; 5000\, \frac{d}{dT}\, \frac{Tw}{5000}$$

or

$$\frac{Q_{IN}}{5000} - \frac{Q_{H_2}}{5000} = MwCpw\, \frac{d}{dT}\, \frac{Tw}{5000} \tag{5-14}$$

$$5000\, \frac{\dot{Q}_{H_2}}{5000} = \frac{\dot{W}}{1}\, Cp\; 5000\, \frac{T_{out}}{5000} - 2000\, \frac{T_{in}}{2000}$$

$$\frac{\dot{Q}_{H_2}}{5000} = \dot{W}\, Cp\, \frac{T_{out}}{5000} - 0.5\, \frac{T_{in}}{2000} \tag{5-15}$$

$$5000\, \frac{T_{out}}{5000} = C_1\; 2000\, \frac{T_{in}}{2000} + C_2\, \frac{Tw}{5000}\; 5000$$

$$\frac{T_{out}}{5000} = 0.4\, C_1\, \frac{T_{in}}{2000} + C_2\, \frac{Tw}{5000} \tag{5-16}$$

In the above analog simulation diagram, time scaling is not yet introduced; any convenient time scale can be used.

where $t_c = \tau.\beta$

t_c = computer time

t = real time

β = time scale

As stated previously, the object of this exercise is to match the results obtained in the digital computer simulation. Since Steps in $\dot{Q}_{IN}$ were considered first, some attention will be given to that aspect of the problem.

Run No.	$\dot{Q}_{IN}$ (Heat Input) Btu/sec	$\dot{W}$ (Flow Rate) lbm/sec
IA	2623	0.420
IB	2623 50/210	0.100
ICa	2623 125/210	0.250
ICb	2623 156/210	0.250
ICc	2623 93.75/210	0.250
IIA	2623	0.462
IIB	2623 50/210	0.110
IICa	2623 125/210	0.275
IICb	2623 125/210	0.225
IICc	2623 156/210	0.275
IICd	2623 93.75/210	0.275

5.2.1.2 Analysis for Step Changes in Heat In ($\dot{Q}_{IN}$)

The time constant of the above closed loop can be obtained by simple algebraic multiplication of the open-loop gains.

$$\frac{1}{\tau} = \frac{C_2 \; W \; C_p}{Mw \; Cpw} \tag{5-17}$$

or

$$\tau = \frac{Mw \; Cpw}{C_2 \; \dot{W} \; C_p} \tag{5-18}$$

As indicated in equation (5-18), for a given $\dot{W}$, t will depend on Mw.

The results of a run are shown below:

For, $\dot{W}$ = 0.42 lbm/sec

$\dot{Q}$ = 2623 Btu/sec

The following values will be set on the various pots shown in Figure 5.2-13.

P30 = 0.525
P07 = 0.4000
P35 = 0.1510
P05 = 0.2220
P32 = ??
Q02 = 0.1560
P11 = 0.0200

Since the normalized computer equations are used, the potentiometer settings are dimensionless.

The value of P32 is yet to be determined.

The response of the outlet temperature was known to be a first-order response; therefore, the value of P32 was obtained as follows. The total mass (fins and the hot skin mass) was given to be 46.6 lbm. It was found that this mass (Mw) 46.6 yielded good results.

In Figures 5.2-14, it is seen that $\dot{W}$ is held constant and $\dot{Q}_{IN}$ is stepped to a given value at time 0. The graphs obtained from the different runs and the digital computer results are given in Figures 5.2-15, 5.2-16, and 5.2-17.

Before concluding the discussion of the response of the system to steps in $\dot{Q}_{IN}$, some interesting observations should be related.

Examination of the time constant of the system revealed that the time constant does not depend on $\dot{Q}_{IN}$, and its relation to $\dot{W}$ will be:

$$\tau = \frac{0.96}{\dot{W}} \qquad (5\text{-}19)$$

The lack of dependence of the time constant from $\dot{Q}_{IN}$ can be seen from the analog computer simulation diagram. This relationship is shown in Figure 5.2-7.

Second, the digital computer results indicate that the wall temperature response has a different time constant from the coolant outlet temperature. The system described previously will yield the same time constant for both temperatures; this will introduce inaccuracies in the wall temperature, a fact which was discussed previously.

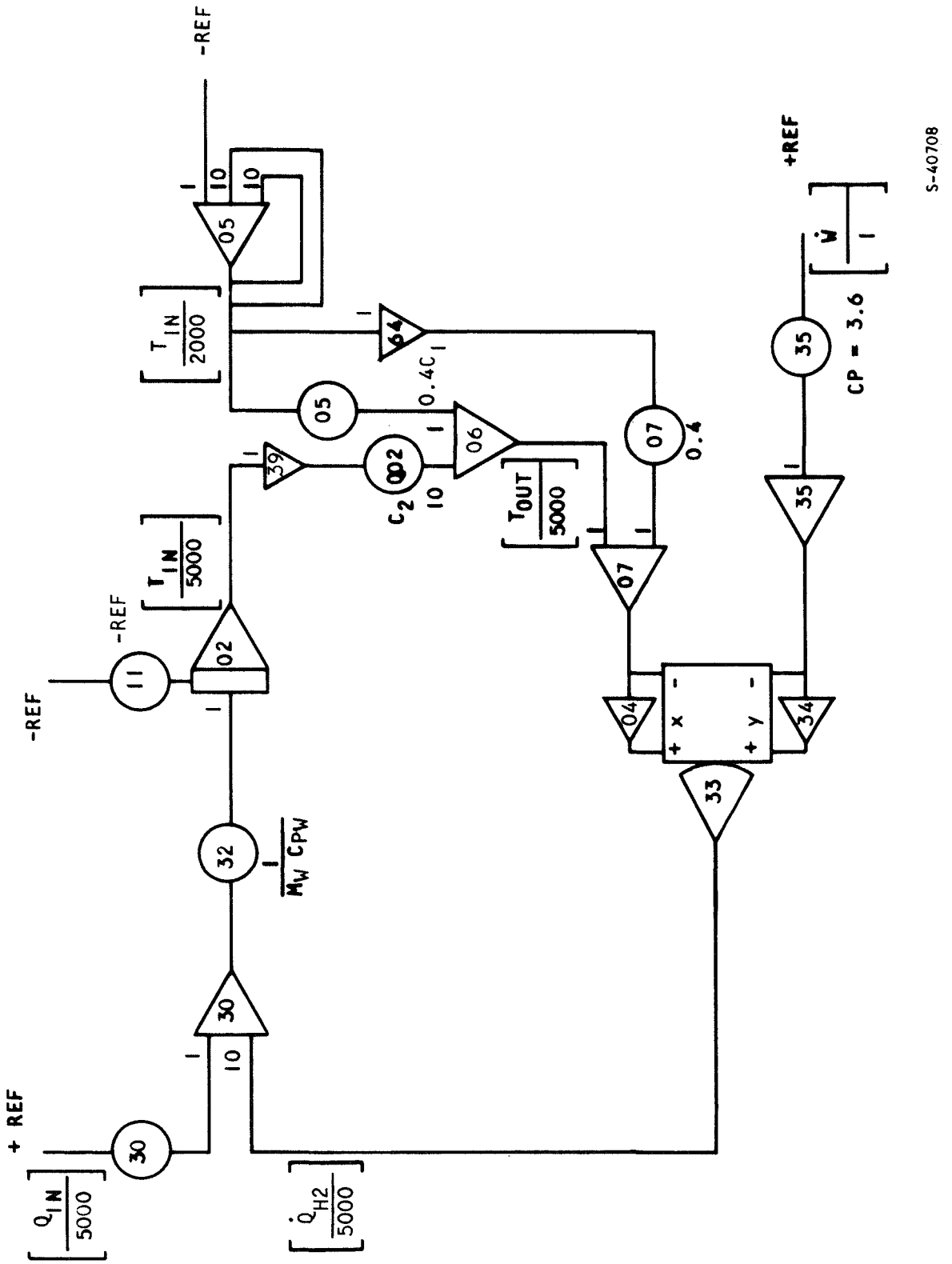

Figure 5.2-13. Analog Computer Diagram for Heat Exchanger

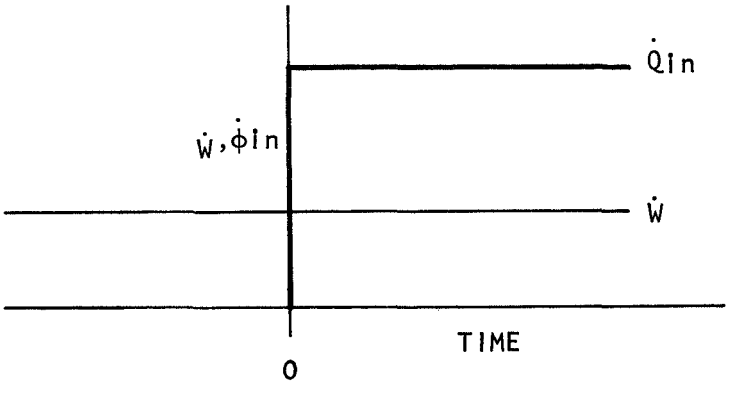

Figure 5.2-14. Representation of Step Changes In $\dot{Q}$

5.2.1.3 Responses to Step Changes in Coolant Flow Rate

The effect of step changes in the flow rate on the system can be expressed by:

$$T_{out} = C_1 T_{in} + C_2 T_w \qquad (5\text{-}20)$$

where $C_1 = \dfrac{2\dot{W} - K\dot{W}^{0.8}}{2\dot{W} + K\dot{W}^{0.8}}$

$$C_2 = \frac{2K\dot{W}^{0.8}}{2\dot{W} + K\dot{W}^{0.8}}$$

If it is assumed that Tw will remain constant for a short time, the immediate effect of a step change in $\dot{W}$ can be calculated by differentiating equation (5-20) with respect to $\dot{W}$.

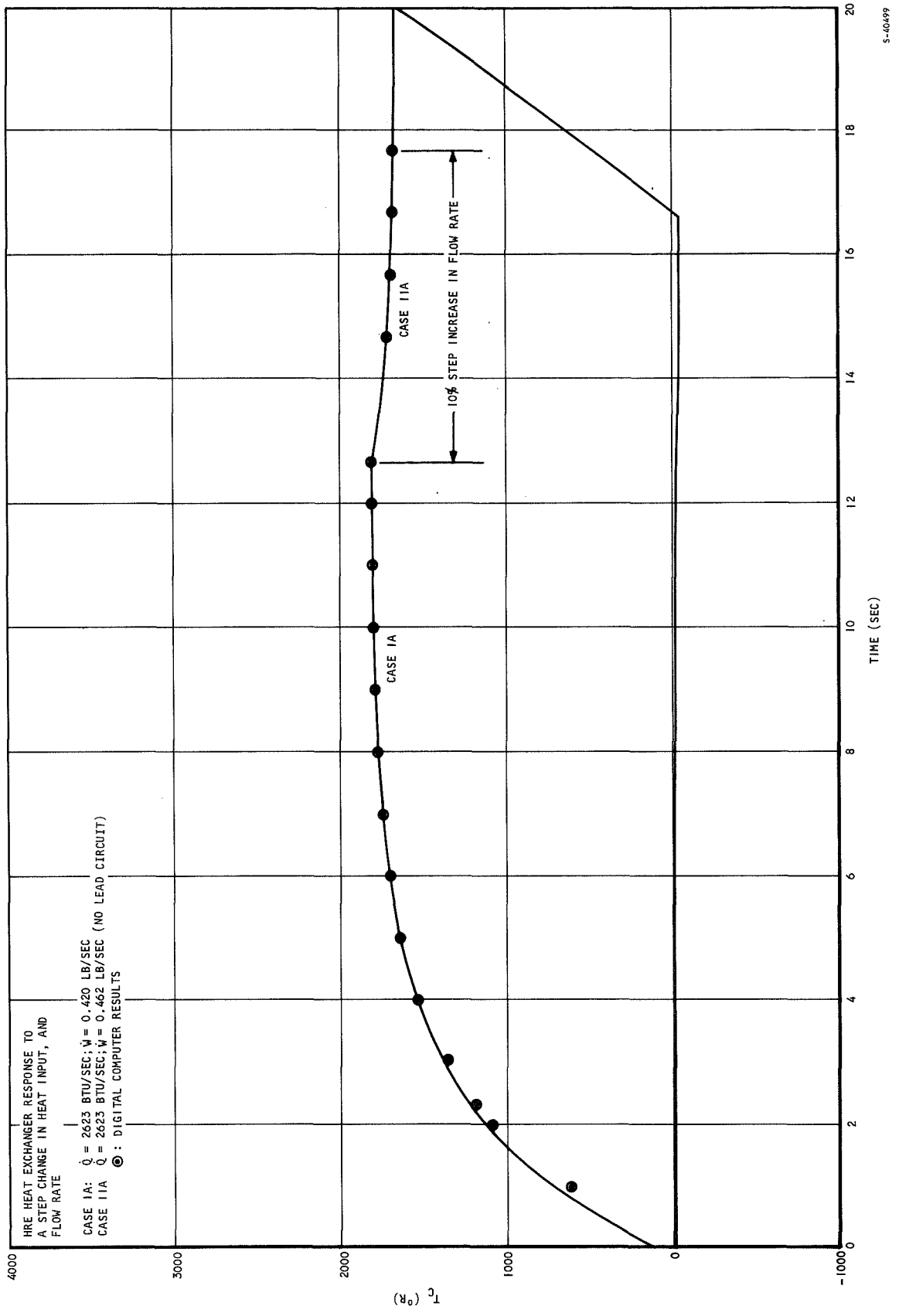

Figure 5.2-15. Case IA and Case IIA

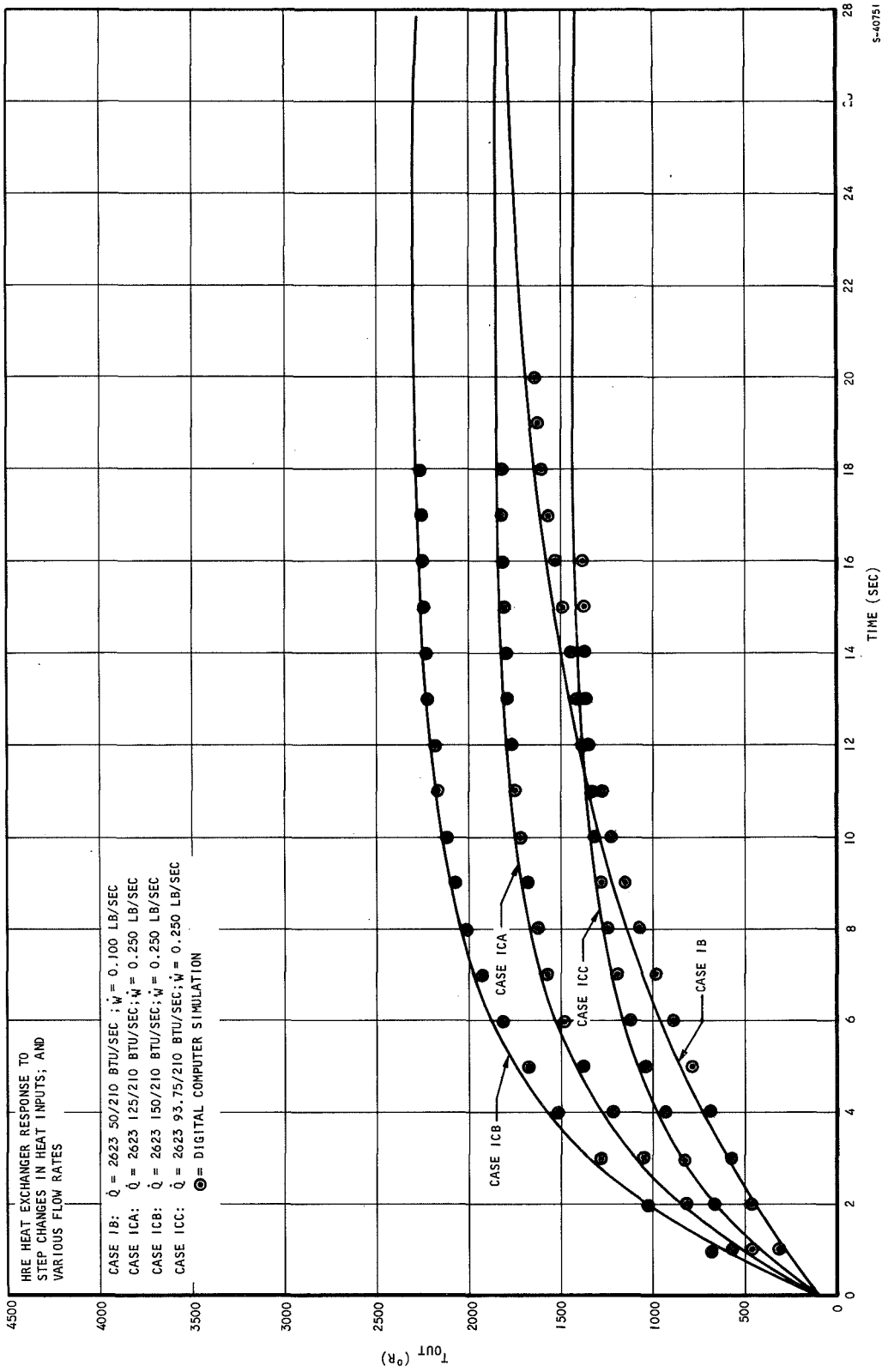

Figure 5.2-16. Cases IB, ICA, ICB, ICC

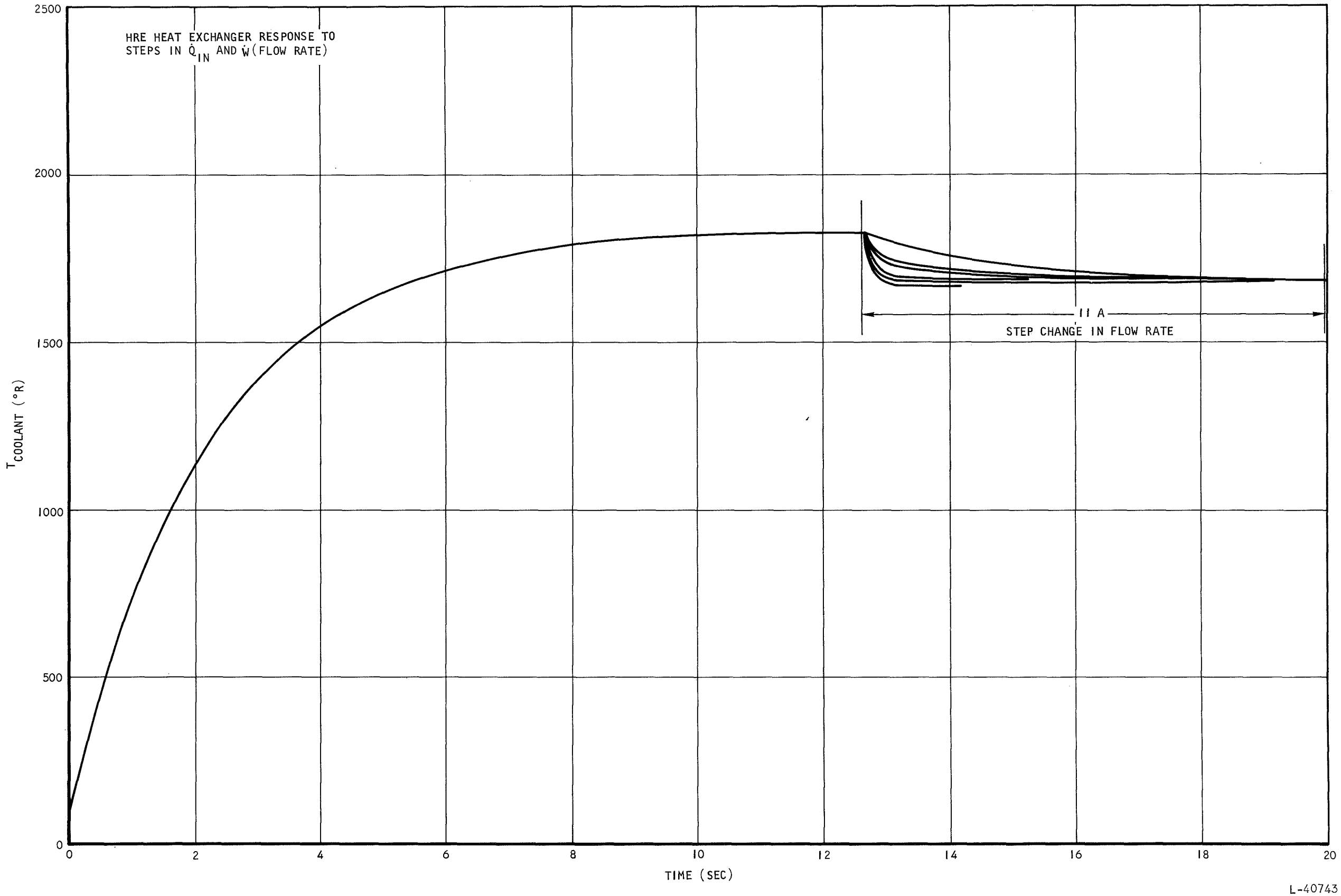

Figure 5.2-17. Cases IA and IIA for Varying β and α

$$\Delta T_{out} + \frac{(2-0.8\,K\,\dot{W}^{-0.2})(2\,\dot{W}+K\,\dot{W}^{0.8})-(2+0.8K\,\dot{W}^{-0.2})(2\dot{W}-K\,\dot{W}^{0.8})}{(2\,\dot{W}+K\,\dot{W}^{0.8})\,2}$$

$$+\frac{(1.6\,K\,\dot{W}^{-0.2})(2\,\dot{W}+K\,\dot{W}^{0.8})-(2+K\,0.8\,\dot{W}^{-0.2})(\dot{w}\,K\,\dot{W}^{0.8})}{(2\,\dot{W}+K\,\dot{W}^{0.8})\,2}Tw \qquad (5\text{-}21)$$

or

$$\Delta T_{out} + \frac{4\dot{W}+2K\,\dot{W}^{0.8}-1.6\,K\,\dot{W}^{0.8}-0.8\,K\,\dot{W}^{0.6}-4\,\dot{W}+2K\,\dot{W}^{0.8}=16\,K\,\dot{W}^{0.8}+0.8\,K\,\dot{W}^{0.6}}{(2\,\dot{W}+K\,\dot{W}^{0.8})\,2}$$

$$+\frac{3.2\,\dot{W}^{0.8}+1.6\,K\,\dot{W}^{+0.6}-4\,K\,\dot{W}^{0.8}-1.6\,K\,\dot{W}^{0.6}}{(2\dot{W}+K\,\dot{W}^{0.8})\,2}\,Tw$$

or

$$\Delta T_{out} = \frac{3.2\,\dot{W}^{0.8} - 4\,K\,\dot{W}^{0.8}}{(2\,\dot{W}+K\,\dot{W}^{0.8})\,2}\,(Tw - T_{in}) \qquad (5\text{-}22)$$

Equation (5-20) incorporating the effect of the changing $\dot{W}$ can be expressed as

$$T_{out} = C_1\,T_{in} + C_2\,Tw + C_3'\,(Tw - T_{in})\,\Delta\dot{W} \qquad (5\text{-}23)$$

where $$C_3' = \frac{3.2\,\dot{W}^{0.8} - 4\,K\,\dot{W}^{0.8}}{(2\,\dot{W}+K\,\dot{W}^{0.8})\,2} \qquad (5\text{-}24)$$

From equation (5-20) Tw can be calculated in terms of T_{out} and T_{in}.

$$tw = \frac{(2\,\dot{W}+K\,\dot{W}^{0.8})\,T_{out} - (2\,\dot{W}-K\,\dot{W}^{0.8})\,T_{in}}{(2\,K\,\dot{W}^{0.8})} \qquad (5\text{-}25)$$

Substituting equation (5-25) into (5-23) one will get:

$$= \frac{3.2\,\dot{W}^{0.8} - 4\,K\,\dot{W}^{0.8}}{(2\,\dot{W}+K\,\dot{W}^{0.8})\,2}\;\frac{2\,\dot{W}\,(T_{out} - T_{in}) + K\,\dot{W}^{0.8}\,(T_{in} + T_{out})}{2\,K\,\dot{W}^{0.8}}$$

$$= \frac{3.2\,\dot{W}^{0.8} - 4\,K\,\dot{W}^{0.8}}{(2\,\dot{W}+K\,\dot{W}^{0.8})\,2}\;\frac{2\,\dot{W}\,(T_{out}-T_{in})+K\,\dot{W}^{0.8}(T_{in}+T_{out})-T_{in}\,2\,K\,\dot{W}^{0.8})}{2\,K\,\dot{W}^{0.8}}$$

$$\frac{2\,\dot{W}\,(T_{out}-T_{in}) + K\,\dot{W}^{0.8}\,(T_{out}-T_{in})}{2\,K\,\dot{W}^{0.8}}$$

or

$$\frac{3.2\,\dot{W}^{0.8} - 4\,K\,\dot{W}^{0.8}}{(2\,\dot{W} + K\,\dot{W}^{0.8})\,2} \quad \frac{(T_{out})\,T_{in})(2\,\dot{W} + K\,\dot{W}^{0.8}}{2\,K\,\dot{W}^{0.8}}$$

Then equation (5-23) will become,

$$T_{out} = C_1\,T_{in} + C_2\,Tw + C_3\,(T_{out} - T_{in})\,\Delta\dot{W} \tag{5-26}$$

where

$$C_3 = \frac{3.2\,\dot{W}^{0.8} - 4\,K\,\dot{W}^{0.8}}{(2\,\dot{W} + K\,\dot{W}^{0.8})\,2\,K\,\dot{W}^{0.8}} \tag{5-27}$$

This analysis applies for Tw constant, or very short time after the step input in flow rate. Equation (5-26) indicates that for a positive step in $\dot{W}$, there will be a step decrease in T_{out} immediately.

5.2.1.4 The Lead Circuit

To accomplish the desired effect, a transfer function for $\dot{W}$ is devided as follows:

$$\frac{\dot{W}_{out}}{\dot{W}_{in}} = \left(\frac{S + \alpha}{S + \beta}\right)(\beta/\alpha) \tag{5-28}$$

$$\dot{W}_{out} = \beta \int_o^t (\dot{W}_{in} - \dot{W}_{out})\,dt + \frac{\beta}{\alpha}\,\dot{W}_{in}$$

The analog computer diagram for this circuit is shown in Figure 5.2-18.

For $\dot{W}$ constant the integrator input will be zero, and the lead circuit will not affect the results for changes in $\dot{Q}_{IN}$.

For a step increase or (decrease) the following will happened:

$\dot{W} = 0.250$ lbm/sec

$\dot{W}/10 = 0.0250$ lb/sec

The initial condition on the integrator 00 will have to be fixed to have 0.025 comming out of amplifier 41 (A41). This can be done simply by:

$$\beta/\alpha\dot{W} - IC = \dot{W} \tag{5-30}$$

$$IC = \dot{W}\,(\beta/\alpha - 1) \tag{5-31}$$

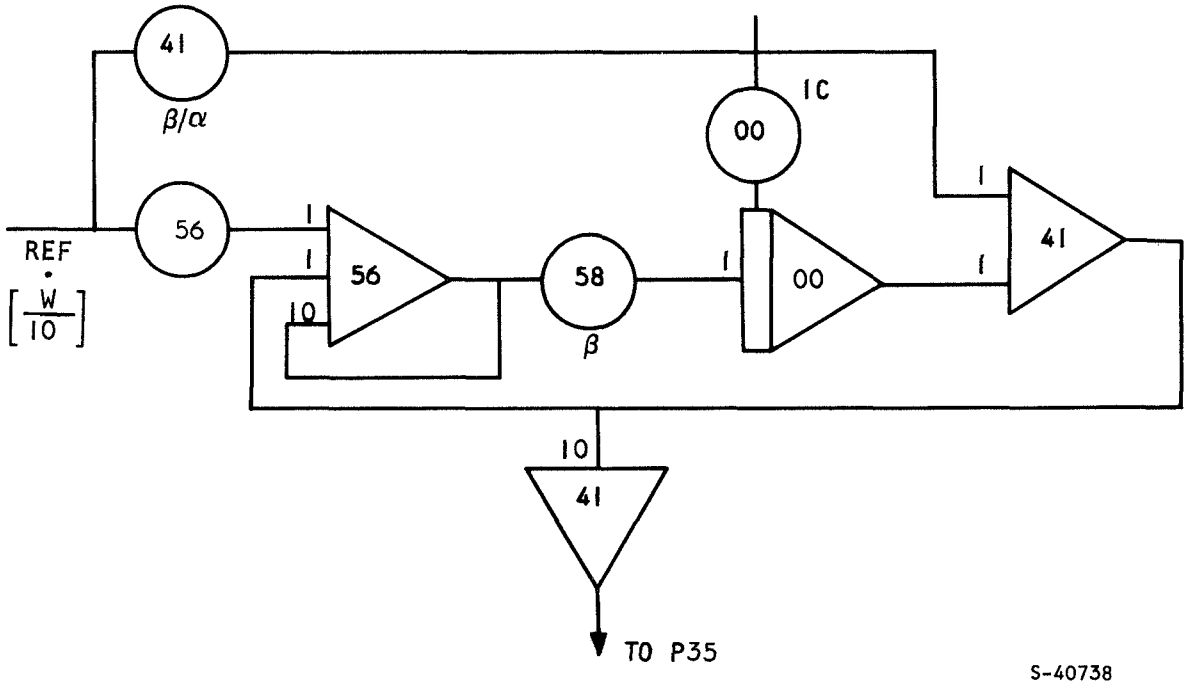

Figure 5.2-18. Analog Computer Diagram for Lead Circuit

for $\dot{W} = 0.025$ and $\beta/\alpha = 5.95$, the IC then is equal to:

$$IC = (4.95)(0.0250) = 0.1239$$

If the flow rate is now increased by a step of 10 percent at time zero the output of amplifier 41 will be:

$$5.95\ (0.0275) - 0.1239 = 0.0397 \qquad (5\text{-}32)$$

Equation (5-32) shows that at time zero rather than having the desired value of 0.0275, as an output of A41, one has 0.0397. Then the input to the integrator will be $+ (0.0397)(\beta/10)$. The integrator will then start to integrate until the desired value of $\dot{W}$ is reached. The speed of integration, of course, depends on β/α, β, and $\dot{W}$. Figure 5.2-19 will further explain the response of $\dot{W}$.

The overshoot in Figure 5.2-19 will depend on α, β, and $\dot{W}$. Then by changing α and β one would be able to get a desired "step" in T74 and since after a short time the lead circuit would stop affecting the time constant, this jump would be followed by a first-order response.

For the case for which is was changed from 0.42 to 0.462 lbm/sec, and $\dot{Q}_{IN}$ held at 2623 Btu/sec very good results were obtained by using $\beta/\alpha = 5.95$ and $\beta = 8.00$. (See Figures 5.2-20, 5.2-21, and 5.2-22.) When this method was applied to different flow rates ($\dot{W}$ between 0.250 to 0.275, or 0.10 to 0.11), it was found that the effective mass would have to be changed to get results similar to the digital computer simulation. Since changing the effective mass of the heat exchanger for different flow rates is not desirable, some other methods were sought.

If, for example, a quantity is equal to $C_3\ \Delta\dot{W}\ (T_{out} - T_{in})$ is subtracted (or added) to A06, a step drop in outlet temperature flowed with a first-order system can be expected. The time constant of this first-order drop would be expected to follow $(0.96/\dot{W})$. However, when the digital computer results were analyzed, it was found that t was no longer equal to $0.96/\dot{W}$, and that a correct response (or matching the results) with the digital computer program was not possible without changing the effective mass.

As has been discussed, simulation of the system response to steps in heat input was not too difficult. For $W \approx 0.45$, this simulation was carried to steps changes in coolant flow rate. However, difficulties arose when an attempt was made to simulate the system response to steps in $\dot{W}$, when $\dot{W}$ is between 0.1 and 0.3 lb/sec.

To find some answers to the above question, the digital computer results are being analyzed carefully.

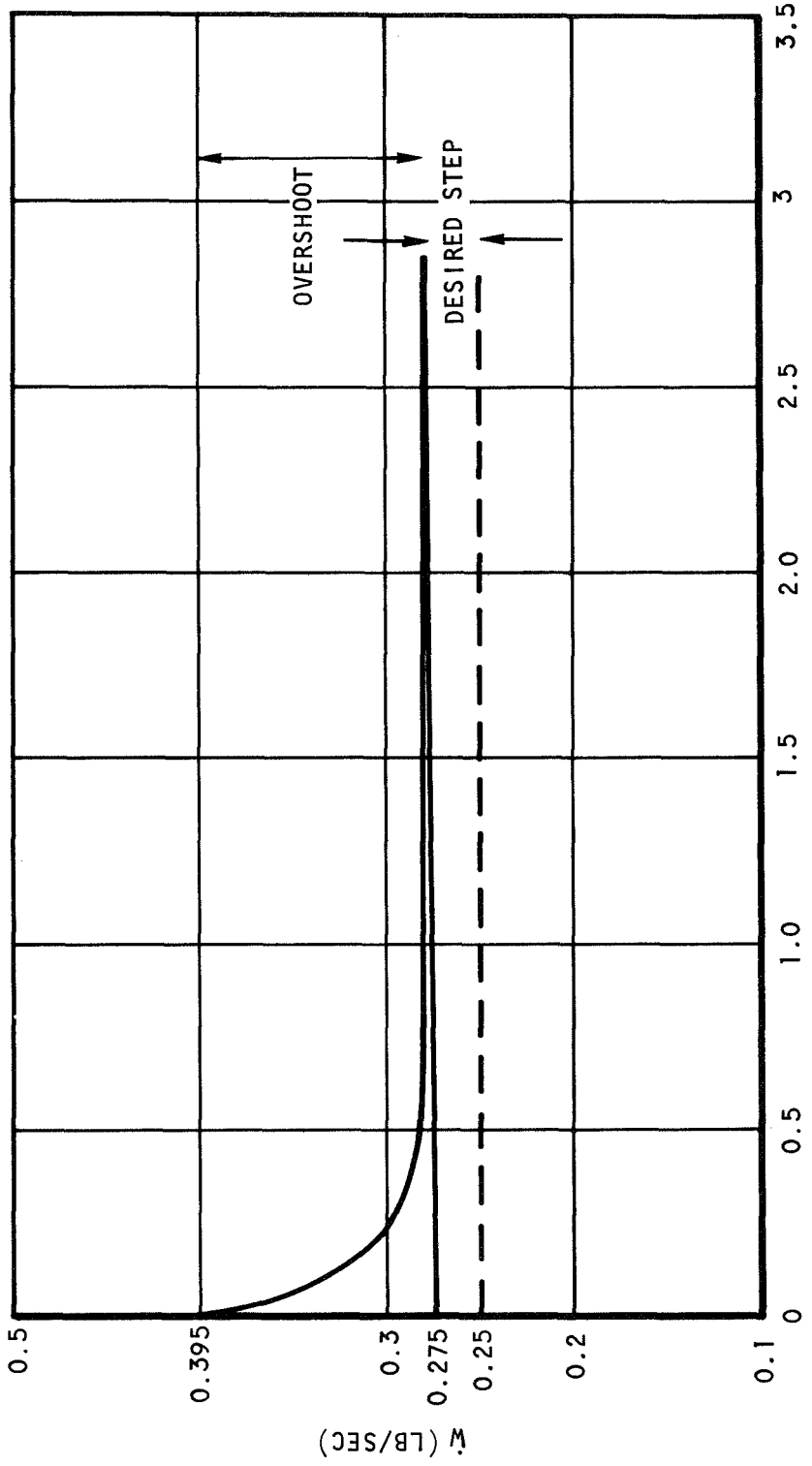

Figure 5.2-19. $\dot{W}$ vs Time Using the Lead Circuit

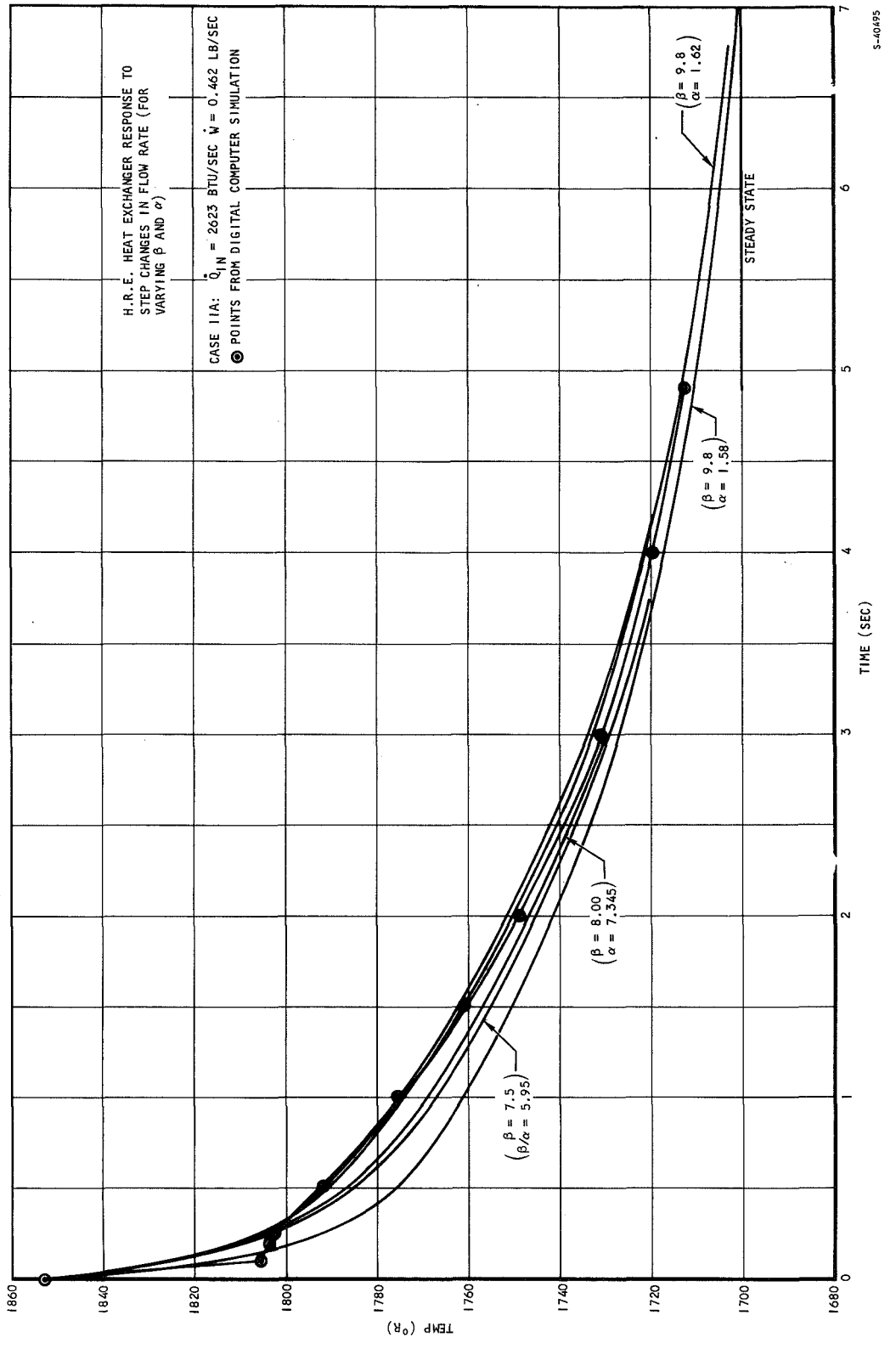

Figure 5.2-20. Case IIA for Varying ρ and α

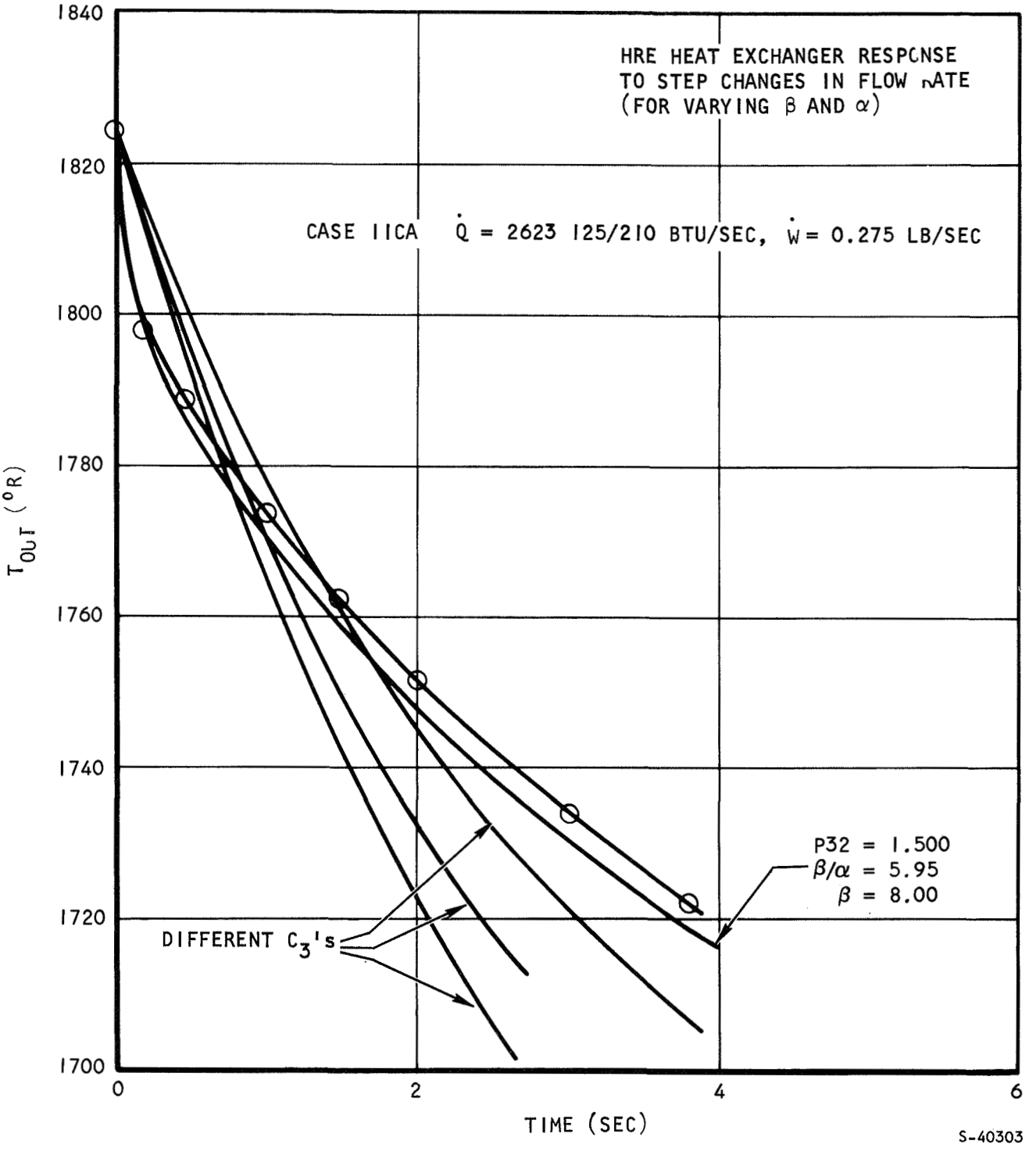

Figure 5.2-21. Case IIA for Varying β/α and C_3

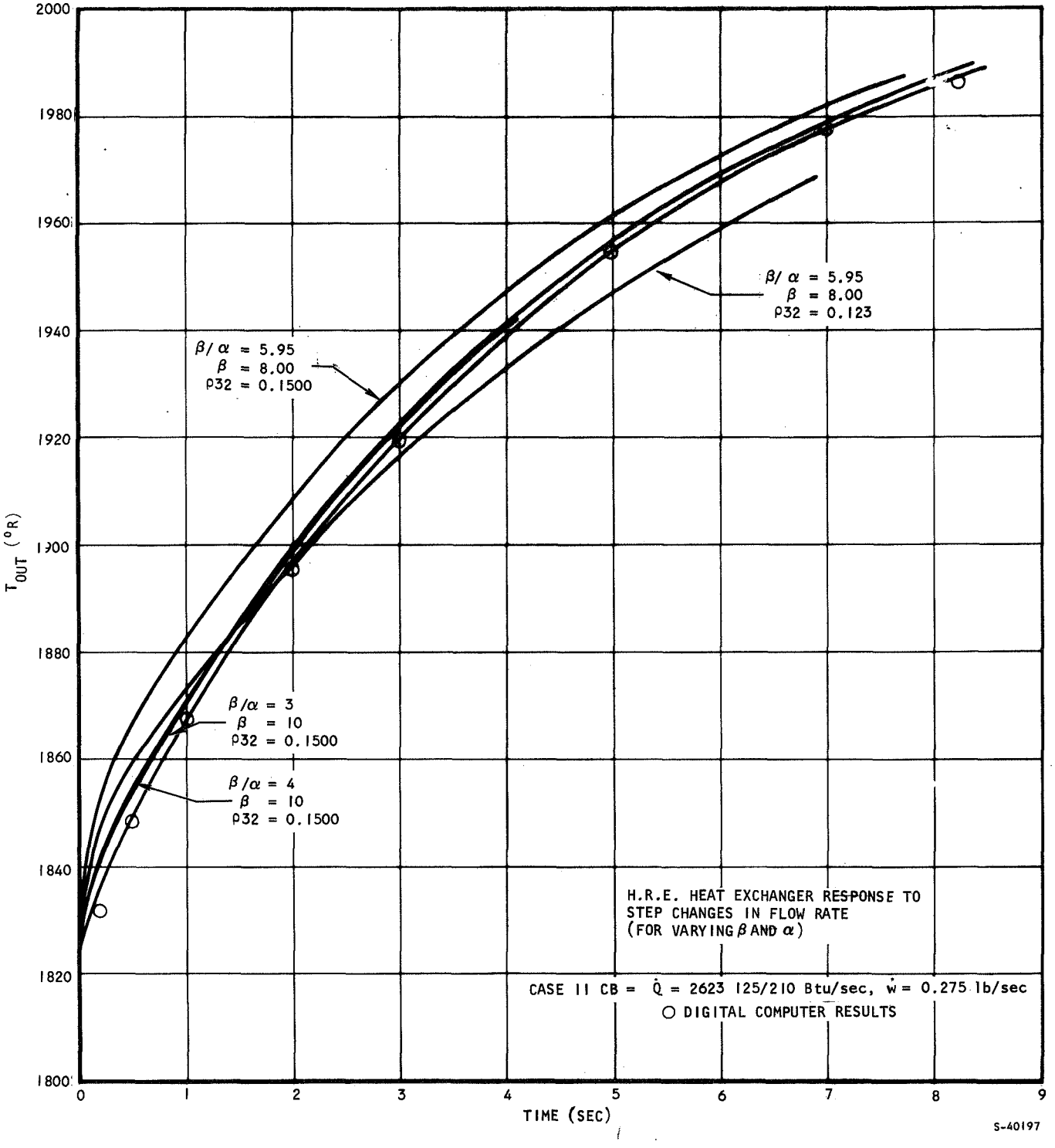

Figure 5.2-22. Case IIA for Varying β/α

The temperature profile for the coolant across the heat exchanger has been plotted. For large T, large heat inputs, they are not straight lines, whereas for small T (small changes in $\dot{W}$ or $\dot{Q}$) the profiles are straight lines. By defining $T_{ave} = \frac{T_{out} + T_{in}}{2}$, it is assumed that the temperature profile is indeed a straight line. Although for transient responses of the outlet temperature for large $\dot{Q}_{IN}$ there will be some error due to approximation of mentioned profiles as straight lines, it is felt that this error is reflected in the wall temperature for the cases where $\dot{Q}$ is changed step-wise. Since, for small changes in $\dot{W}$, the temperature profile is indeed a straight line (or very close to it) the above definition for $T_{H_{2ave}}$ should be true and very small errors should be encountered.

Although no definite program which will yield accurate results for changes both in $\dot{Q}_{IN}$ and $\dot{W}$ has been achieved yet, useful conclusions can still be made. It seems that the main problem is the simulation of the nonlinear response immediately following the step changes in W. It should be remembered that the curves for the temperature response, for step changes in $\dot{W}$, are drawn on an enlarged scale and hence temperature differences on the order of 10 to 20°F appear to be very large errors. From the investigation performed so far, it is felt that point-by-point matchup of the two different computer results is impossible without changing the effective mass of the heat exchanger. There are methods available (using $C_3 \Delta T \Delta\dot{W}$, for example) which will give an immediate step and follow the curve from digital simulation within 20°F after the forementioned step drop. Considering the magnitude of the outlet coolant temperature (on the order of 1100°F) this difference may be acceptable.

5.2.2 Static Tests

The static tests provide steady-state values of pressure and flow for conditions of varying valve areas or injector flow. The test conditions did not necessarily correspond to specific flight conditions, but served more as a test of the validity of the simulator than as a prediction of what will happen in the actual cooling system.

A block diagram of the simulator is shown in Figure 5.2-23. The system is initiated at conditions of Mach 8, B-B flight conditions, with an engine operating ϕ of 1.0. The simulation is operated in a mode that causes the simulator to operate 10 times as fast as the actual cooling system. Any changes in the input variables such as the valve areas will produce immediate steady-state values of the pressures and flows in the system. It is assumed in these tests that the heat inputs (Q_1 through Q_6) increase and decrease as the flows increase and decrease, so that the heat exchanger temperatures remain fixed at their initial values.

A simple control system was included in the simulation, to simulate the effect of the turbopump. This controller increased or decreased turbopump discharge pressure (P_1) to keep main fuel plenum pressure (P_9) constant.

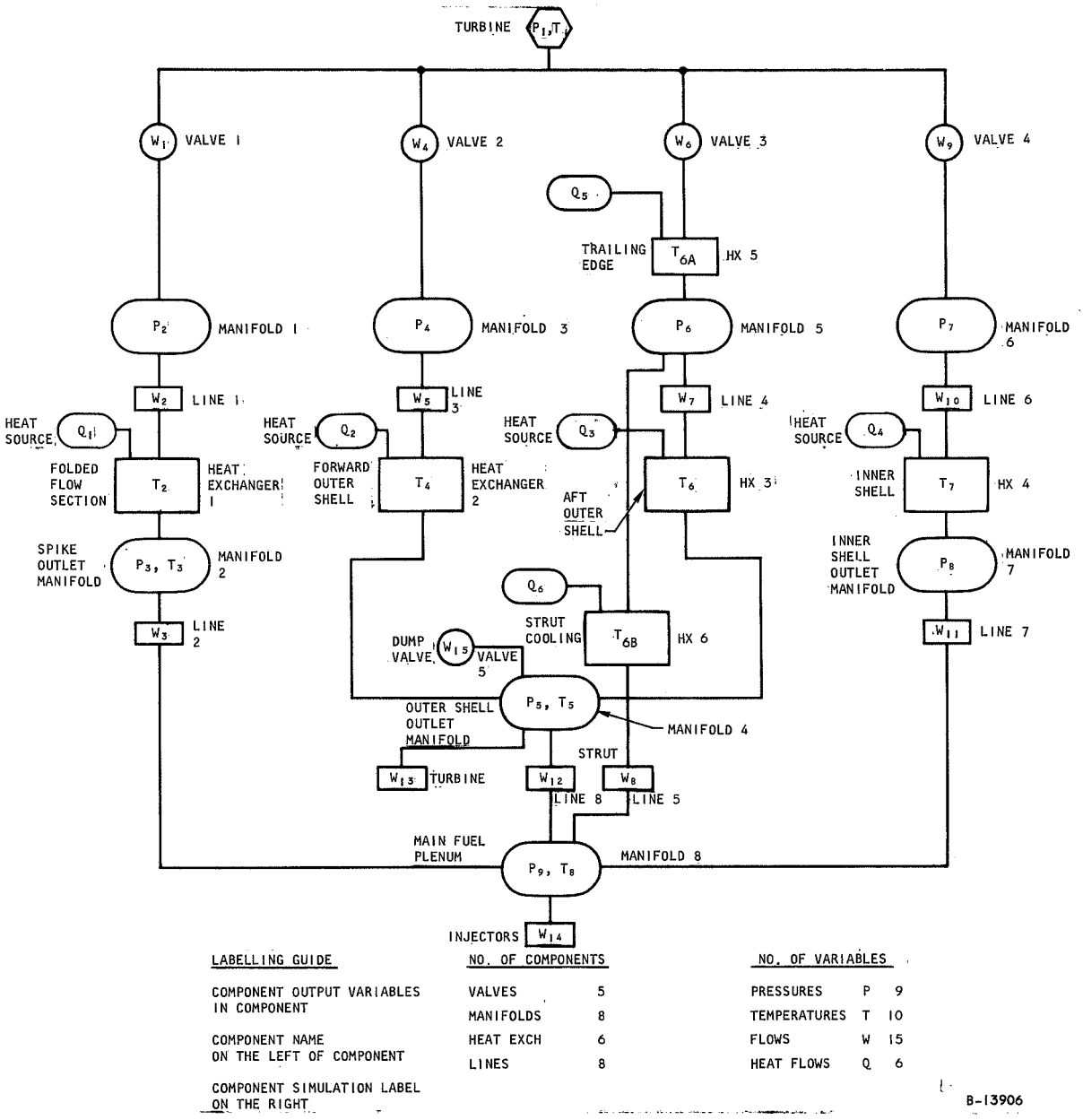

Figure 5.2-23. Heat Exchanger Schematic

The steady-state results for changing dump valve area are shown in Figures 5.2-24 and 5.2-25. The pressures and flows are identified in Figure 5.2-23.

5.2.3 Frequency Response Tests

The purpose of these tests was the acquisition of frequency response data which is pertinent to the temperature controls and the turbopump control. The dynamics of the heat exchanger were not included in these tests. The information pertinent to temperature control is the response of coolant flow through a heat exchanger to changes in the area of the valve which controls its coolant flow. These tests were conducted without the turbopump control system; i.e., turbopump discharge pressure (P_1) is kept at a constant value. This implies that the temperature control system will be considerably faster than the turbopump control system. The validity of this assumption will be examined after the turbopump has been simulated.

The response of the flow through heat exchanger to changes in the upstream valve area (valve 1) is shown in Figure 5.2-26. There are two things particularly noteworthy on the graph. First, the phase lag of the output signal (W_1) has not recorded and second, the slope of the gain fall-off is about 14.4 lb per decade of frequency. Both of these characteristics depend on the type of nonlinearities to be found in the simulation. The only nonlinearities in the system which affect flows and pressures are found in the valves and lines. The equation for flow through a valve is:

$$W = \frac{C_2 P_u A_v N}{\sqrt{T}}$$

where W = flow (lb/sec)

C_2 = valve constant (or/sec)

P_u = upstream pressure (psi)

A_v = effective valve area ($in.^2$)

N = the ratio of unchoked flow to choked flow (as nonlinear function of upstream and downstream pressure)

T = upstream temperature (^0R)

The equation for flow through a line is:

$$W = K \left[P_u^2 - P_D^2 \right]^{1/2}$$

where P_D = downstream pressure (psi)

K = line constant ($in.^2$/sec)

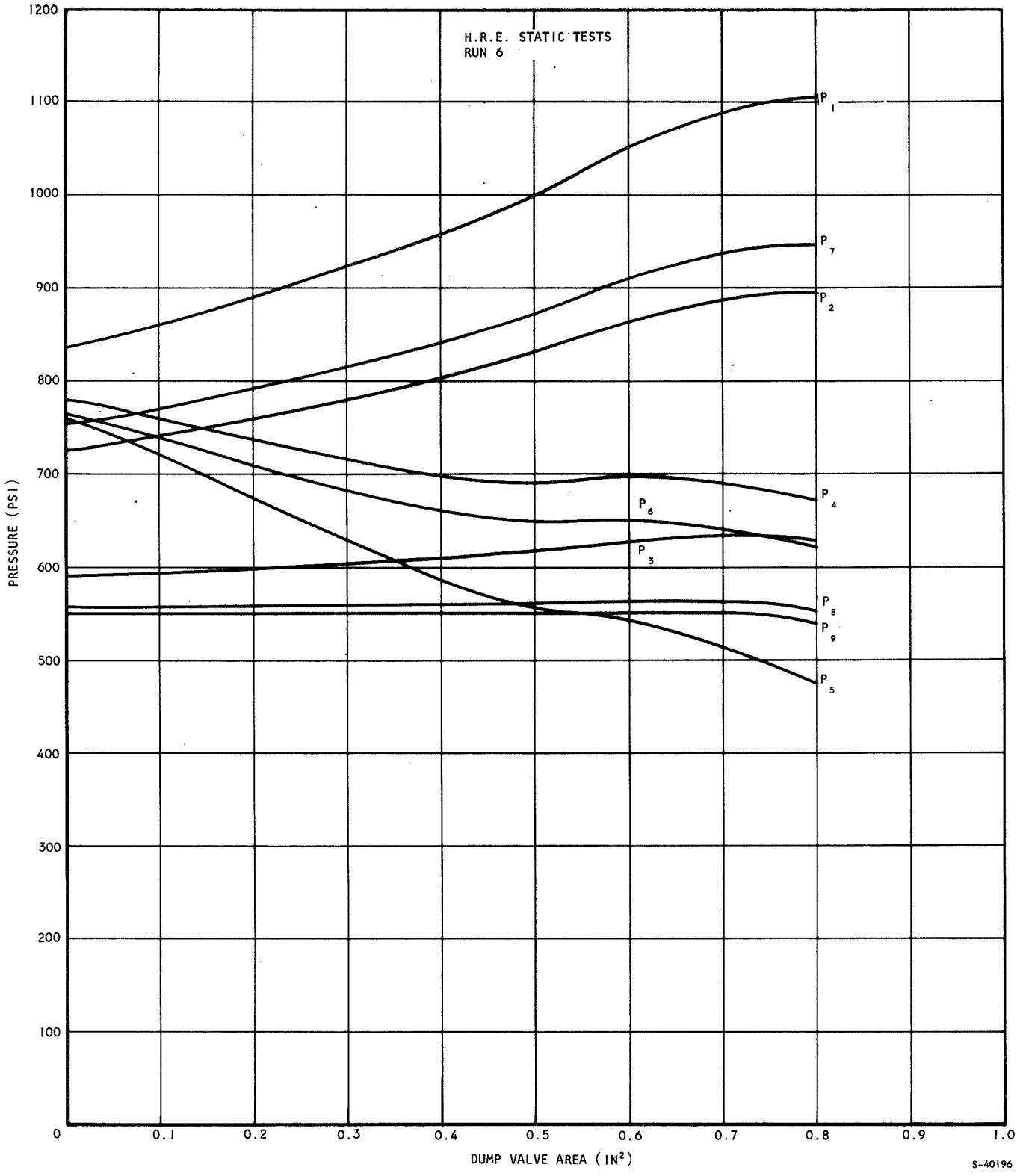

Figure 5.2-24. Steady-State Pressures.

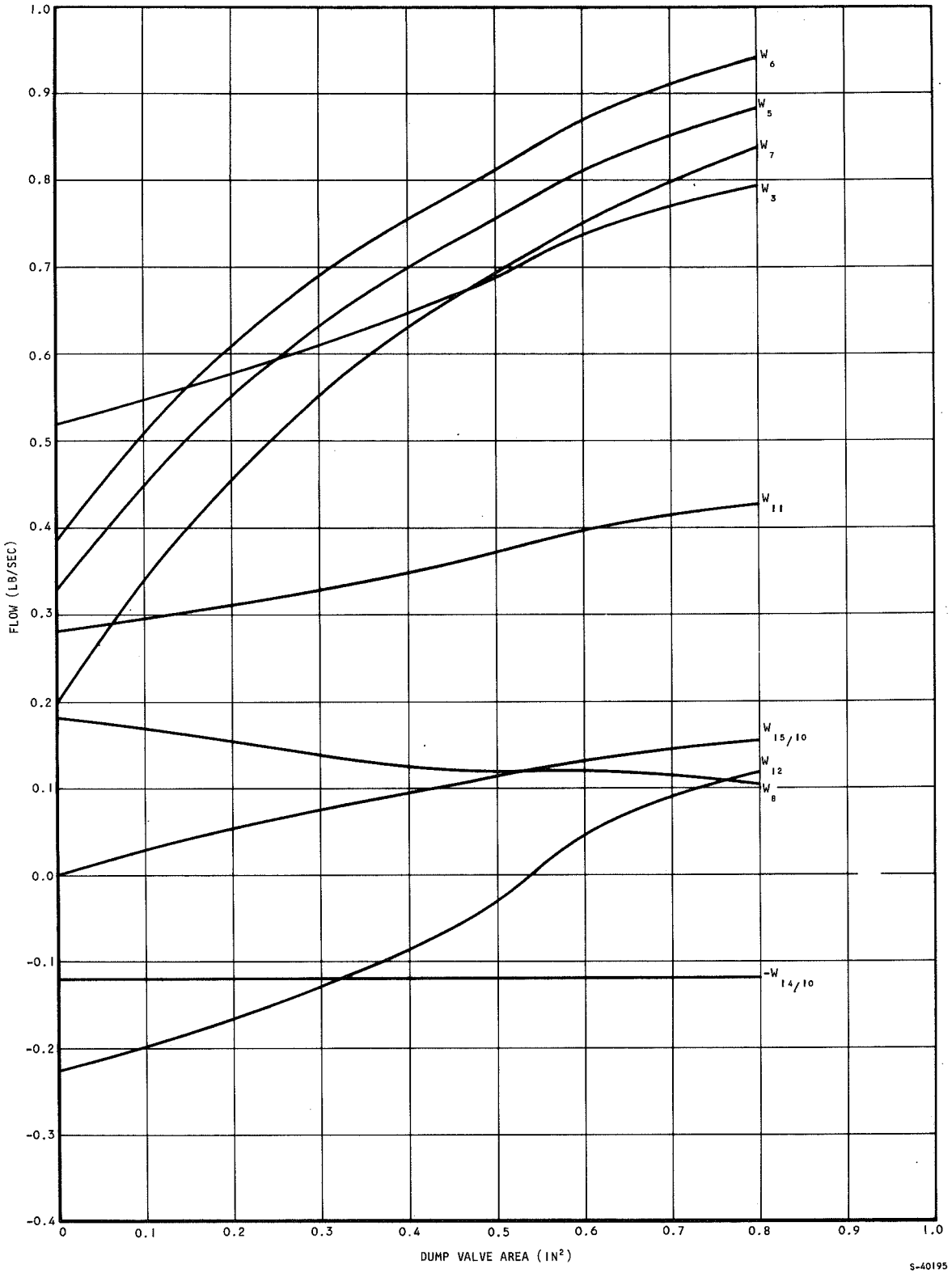

Figure 5.2-25 Steady-State Flows.

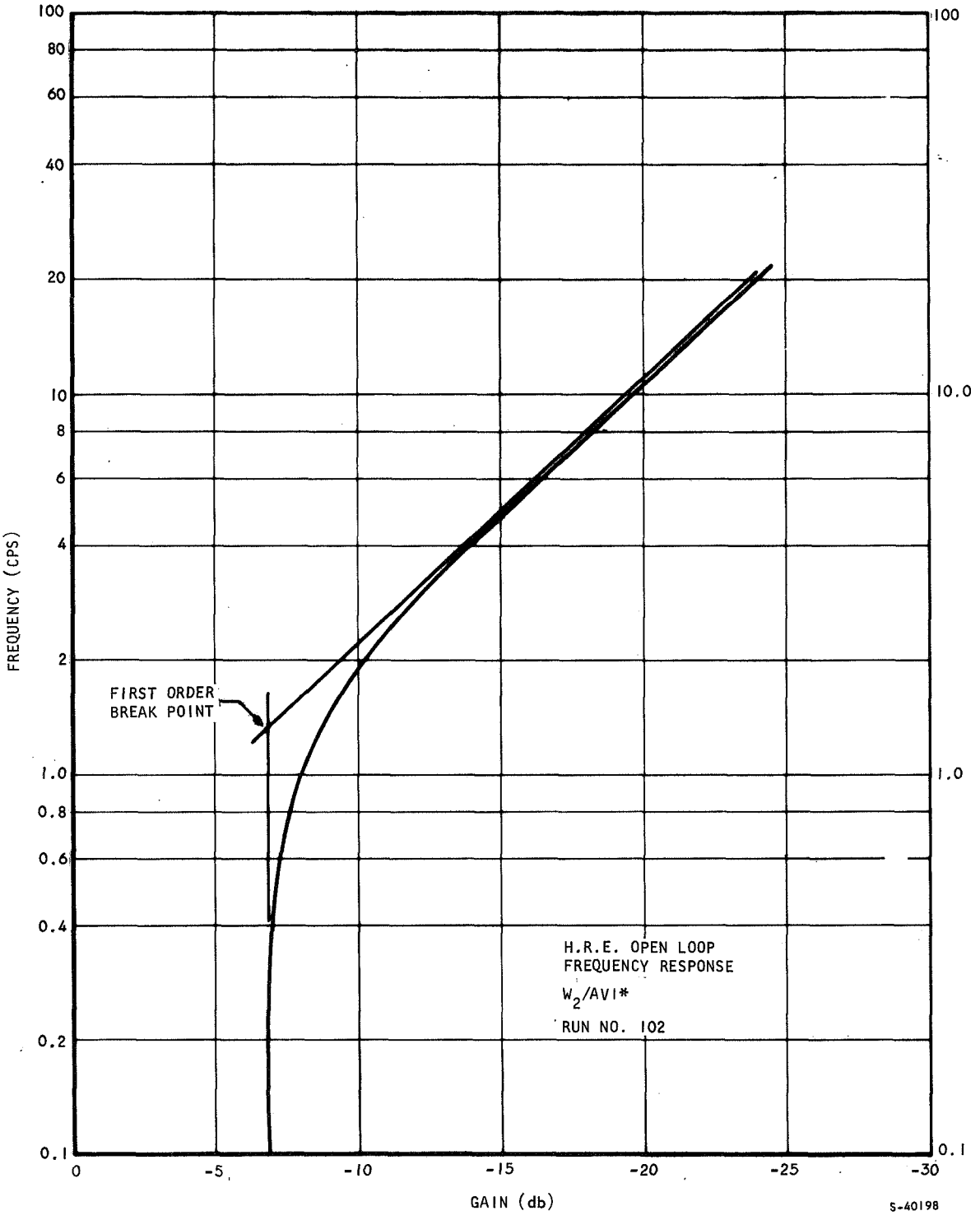

Figure 5.2-26. Frequency Responses.

The important thing about these equations is that they are not differential equations. A change in up or downstream pressure will cause an immediate change in the flow through the valve. Therefore, these nonlinearities do not add any phase lag to the flow signals that are generated by changing pressures on valve areas. Hence, the phase of the response signals will be related to the gain of the response signals exactly as they would be for a completely linear system. That is, the phase is almost zero for a zero slope, it is almost 90^0 after a first order break point, etc.

The gain rolloff of a linear system, after a first-order breakpoint, is expected to be 20 db per decade of frequency. That the measured gain does not follow this pattern is due again to the nonlinear gains of the lines and valves. The gains for these frequency response runs were measured by driving the valve areas with a sinusoidal voltage about their steady-state positions and measuring the amplitude of the resultant oscillations of the flow through the heat exchanger. The ratio of the amplitude of the output oscillation to the amplitude of the input oscillation is the gain for that operating point and frequency. The gains of the valves and lines are independent of the frequency of the driving signal; they depend on the operating point. As the upstream pressure of a valve or line increases, the gain of the device decreases. (For the valves, this is only true if the flow through the valve is unchoked.) A decrease in downstream pressure will have a similar effect. The response of the manifold pressures to changing input and output flows is frequency dependent, and will decrease as the frequency of the flows increase. This decrease in the size of the pressure oscillations causes changes in the effective gains of the valves and lines. In the case of Figure 5.2-26 (the response of flow through heat exchanger 1 to changes in the area of valve 1), the decrease in the size of the pressure oscillation in manifold will cause an increase in the effective gain of line 1 and an increase in the effective gain of the valve. This effect would be nonexistent if infinitesimal driving signals were used, and infinitesimal output oscillations were measured. The fact that the gain fall off has a slope of 14.4 db per decade is not, then, relevant to the study, since, the particular slope which occurs will depend on both the operating point and the amplitude of the input signal. Its only relevance lies in the face that it indicates the presence of a first order breakpoint in the response at about 1.3 cps. This implies that the response has a time constant of about 0.123 seconds.

The gain figures shown are the gains for the analog signals rather than the actual system gains. To relate these gains to actual gains, the scaling of the simulator must be taken into account. For instance,

$$\frac{dW_2}{dA_v} = \frac{dW_2}{\frac{dA_v}{A_{vmax}}} \frac{1}{A_{vmax}} = \frac{dW_2}{A_{v*}} \cdot \frac{1}{A_{vmax}}$$

Since the maximum valve area for valve 1 is 0.07 in., the actual system gain can be computed from the graphed gain by adding:

$$20 \log \frac{(W_2)}{A_v} = 20 \log \frac{(W_2)}{A_v^*} + 20 \log\left(\frac{1}{0.07}\right)$$

$$20 \log \frac{W_2}{A_v^*} = 20 \log \frac{(W_2)}{A_{v1}^*} + 23.1 \text{ db}$$

The steady-state gain is therefore about 16.3 decibels.

If the turbopump was controlled to maintain a constant pressure in the main fuel plenum, the response data which would be most pertinent to the determination of the stability of the control would be the response of main fuel plenum pressure to changes in turbopump discharge pressure. This data is shown in Figure 5.2-27. In this case, both pressures have the same scaling so the gain figures are those which would be expected from the actual system. This data is unrealistic in the sense that the valves all had fixed positions while this data was taken. The influence of the temperature controls will necessarily have to be taken into account in determining the system response which applies to the turbopump control.

All frequency response data were obtained through the use of peripheral analog circuitry, which is described in Appendix B. The validity of the results of this circuitry has been checked with hand calculations, and strip chart recordings of all runs were taken.

5.2.4 Closed-Loop Tests

These tests were undertaken to determine rough design data for the design of the breadboard temperature control circuits. As such, the results of these studies should be numbers for the gains of each of the temperature control loops, type of compensation for the controls, and the expected values of the compensation elements. To obtain this information, several assumptions were made. Since no adequate model of the turbopump was available, it was assumed that the temperature controls would be faster than the turbopump control and, therefore, the turbopump discharge pressure was held at a constant value. To further simplify the study, interaction between the temperature controls was neglected; that is, all of the other valve areas were kept at a constant value. The study was conducted at Mach 8, B-B flight conditions, with an engine ϕ of 1.0. The response used as a standard was the response to a 10-percent step increase in heat input to the heat exchanger. The size of the step is arbitrary and was chosen on the basis of it not leading to amplifier overloading problems. The innerbody flow route was chosen for the study. This choice was based on the availability of an accurate heat exchanger model for this flow route.

The present system proved to be much more controllable than the one studied in the "Interim Heat Exchanger Study." This study is described in the second and third Technical Data Reports. The reasons for this lie in the faster temperature sensing which is now available and the faster response of the flow control valves.

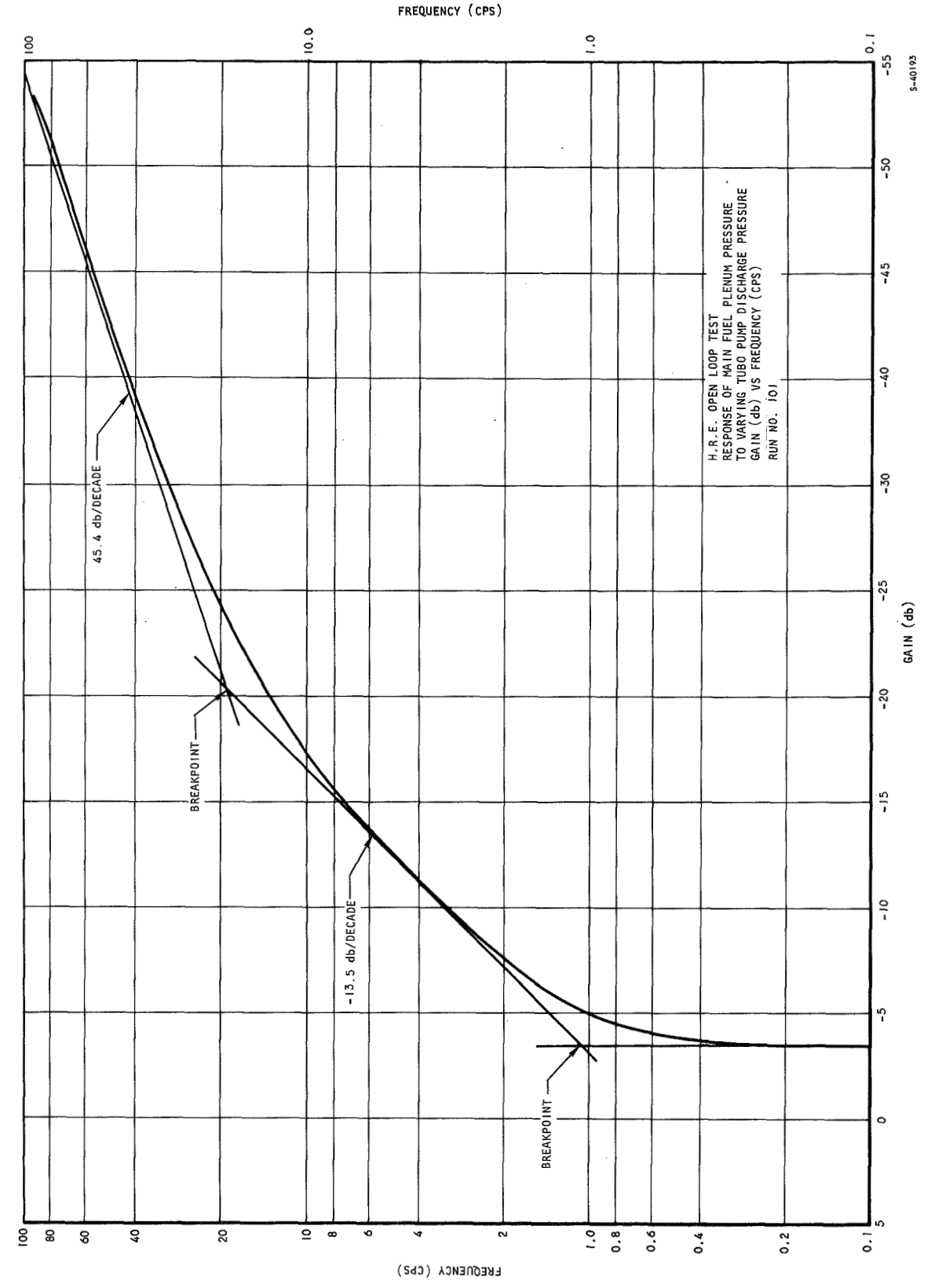

Figure 5.2-27 Frequency Responses of Fuel Plenum Pressure to Turbopump Discharge Pressure.

The result of the study has been the development of a versatile digital compensator which would provide satisfactory system stability for open-loop gains as high as 90. The 10-percent step in heat input to the system would if uncontrolled, cause a coolant temperature rise of about 150°R. The temperature control is able to limit the coolant temperature rise to about 12°R (worst case) and at best to about 2°R in steady state, with about 2°R of overshoot. The settling time is on the order of 1 sec.

5.2.4.1 Temperature Control System Description

A schematic of a typical temperature control is shown in Figure 5.2-28. Each temperature control will receive a number of biased temperature signals from which it will select the highest. This signal will be used to control the corresponding flow control valve.

The function of the select highest device necessitates inclusion of a time delay in the system. If eight temperature signals are to be sampled and if the fourth signal is the highest, the select highest device will have to test the remaining four signals before determining that the fourth signal is the highest. The highest signal is in this case, subjected to a delay of about one half of the sampling period; that is, if all signals are sampled every T seconds, the fourth signal will be delayed by T/2 seconds. The longest delay would occur if the first signal was the highest in which case the delay would be almost the full T seconds (depending on the rise time of the sampling circuitry).

A schematic of the simulated innerbody flow route and temperature control is shown in Figure 5.2-29. Biasing of the temperature signal will, in the hardware system, take place in the cold junction compensators. The select highest circuitry and the sample and hold are simulated by two track and store amplifiers in series. A computer-supplied timer controls these amplifiers. The timer emits a pulse every 1/10 sec. Since the simulator model is slowed down by a factor of 100, the clock emits the equivalent of 1000 pps. The delay feature of the select highest device is implemented by having the second track and store go into track mode first, for one timer pulse, and then go into store while the first track store amplifier goes into track mode for one count. The t and s amplifiers have bandwidths of at least 250 kH in track mode, so that one timer pulse is easily long enough for them to follow the input signal under any conceivable conditions. After the t and s amplifiers have tracked, the timer counts to a predetermined number and then starts the cycle over again. Figure 5.2-30 shows a test run for the track and store devices. The total timer count is 100, which corresponds to sampling once every 10 sec, or, in real time, 10 times a second. The large rise time and overshoot of the steps is due to the relatively poor response of the X-Y plotter. Comparison of the input and output graphs shows that the value held by tank and store amplifier No. 2 is the input delayed by almost exactly 10 sec. Figure 5.2-31 shows the performance of the two track and store amplifiers for a total count of 10. This implies sampling every second, or, in real time, 100 times a second. Under these circumstrances, the time which the computer spends with one or the other of the track and store amplifiers in track mode is no longer negligible. A comparison of input and output shows

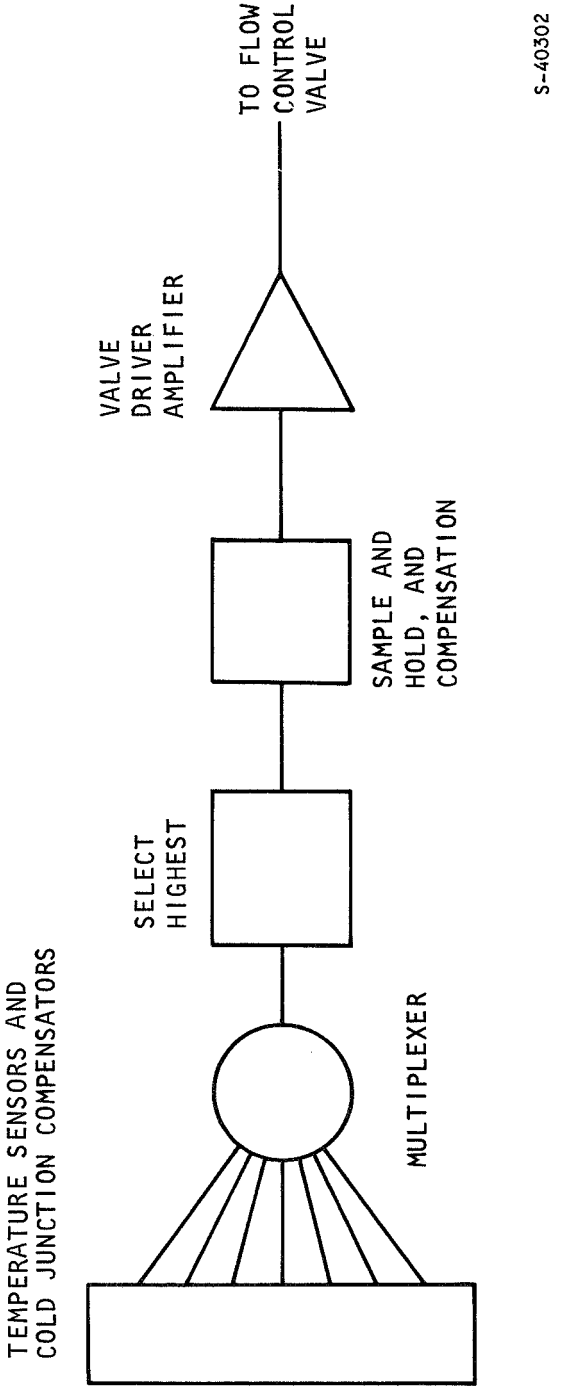

Figure 5.2-28. Temperature Control Schematic

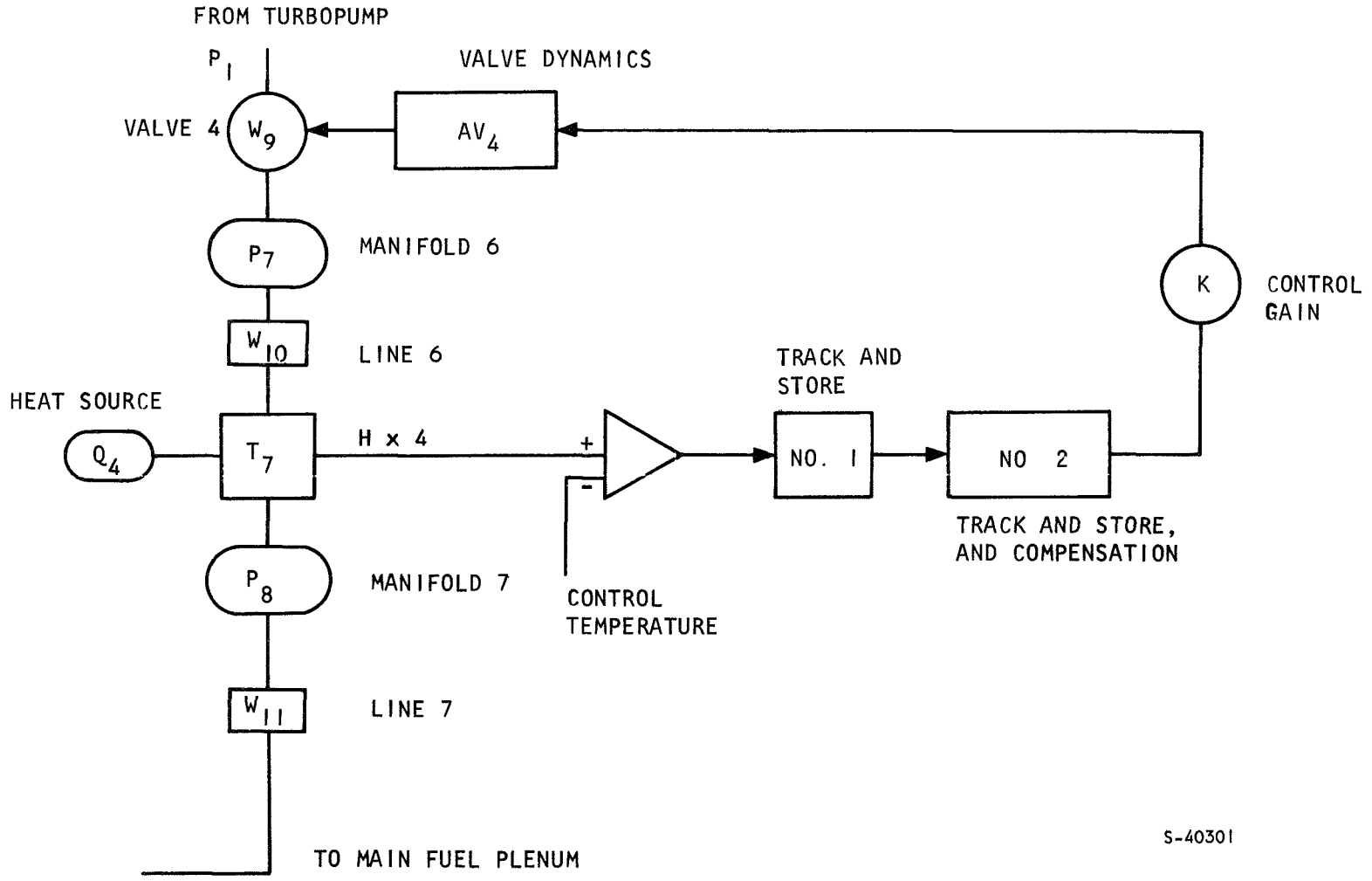

Figure 5.2-29. Innerbody Flow Route and Temperature Control

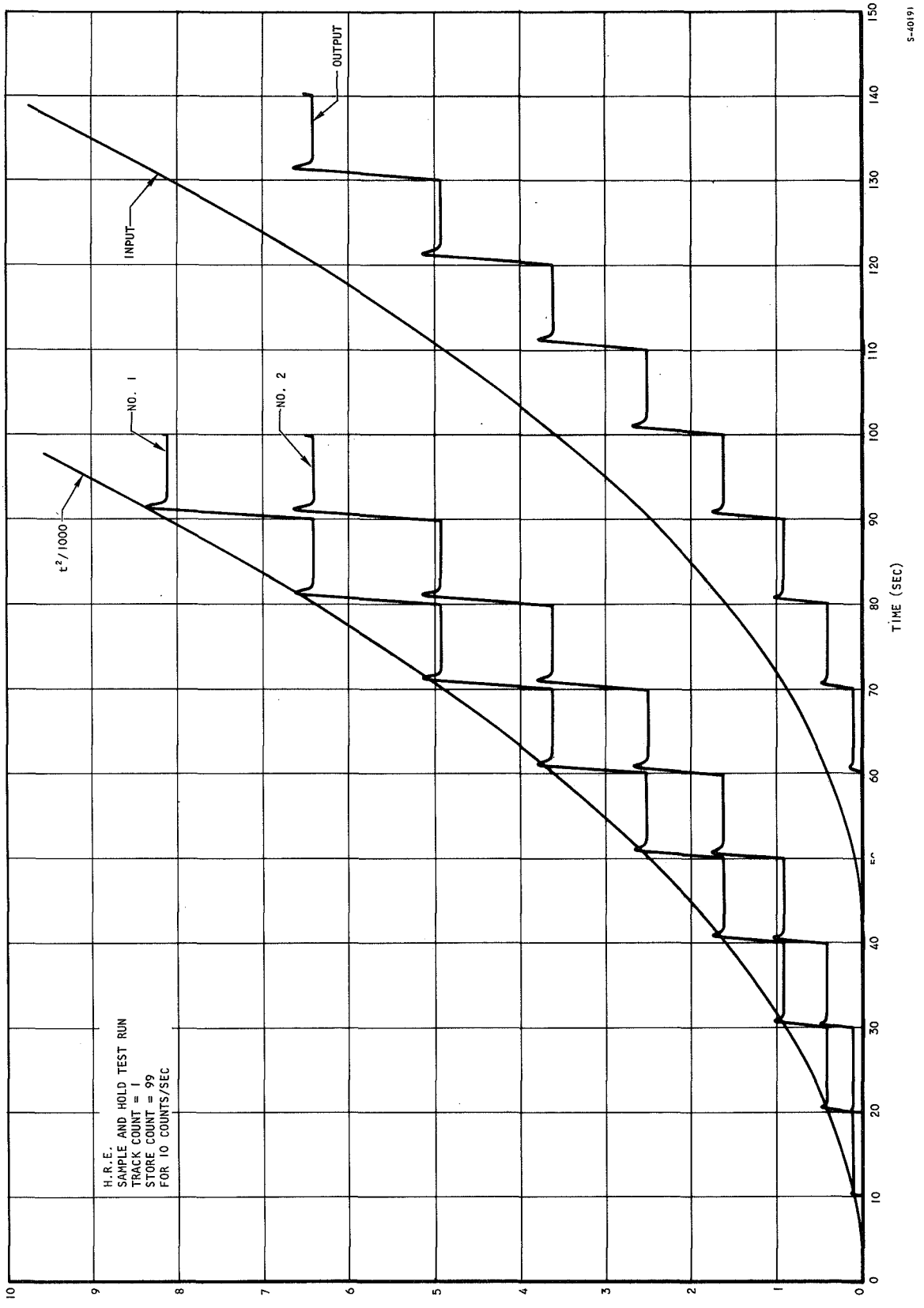

Figure 5.2-30 Track and Store Test; Total Count = 100.

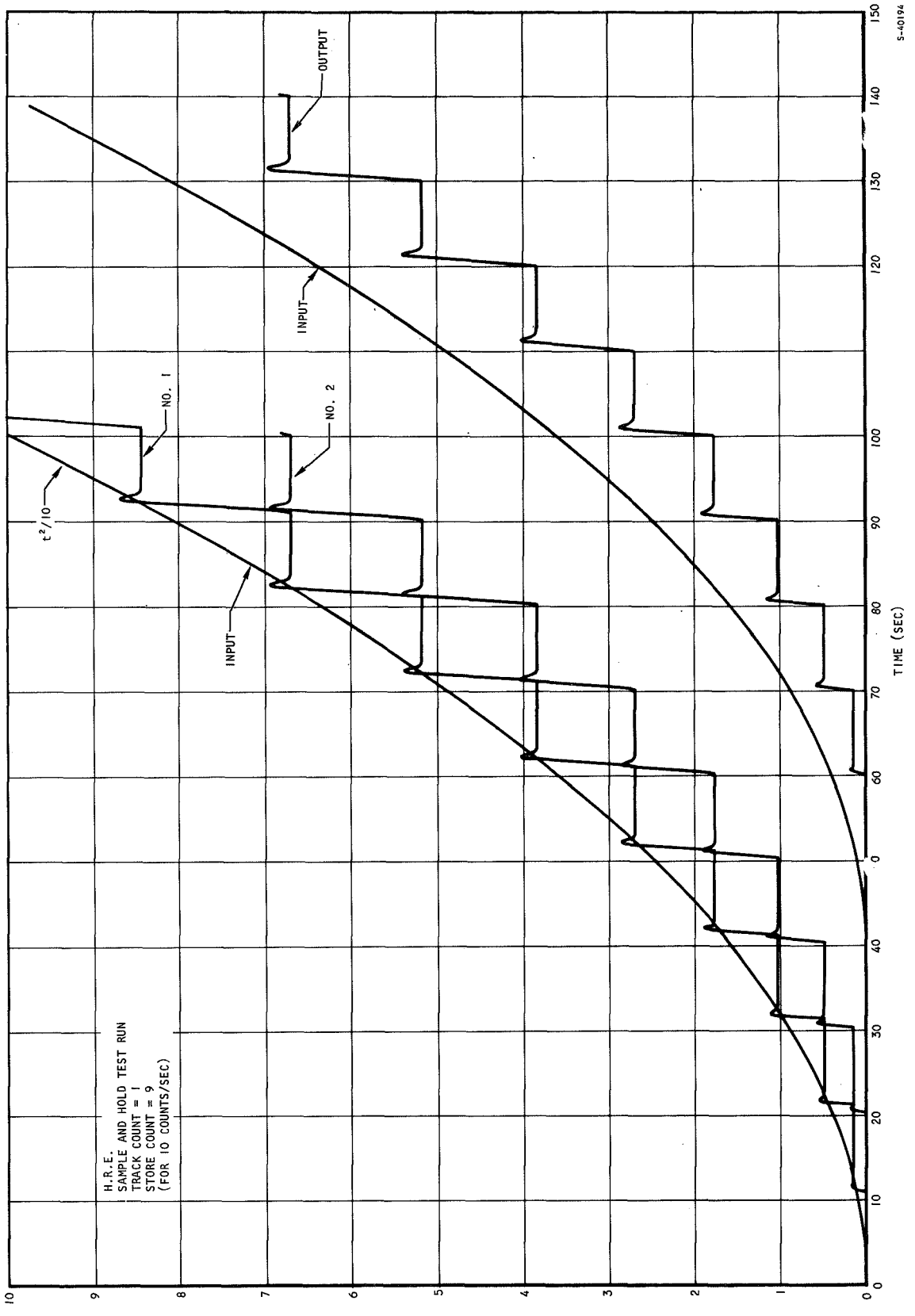

Figure 5.2-31 Track and Store Test; Total Count = 100.

that the output is now delayed by only 0.8 sec (0.08 sec real time). The inaccuracy is acceptable at present.

The valve dynamics are again characterized by a single time constant, of 0.08 sec. This implies a bandwidth of about 2 cps. The valve pneumatic resonance is not included in the valve dynamics. Although the frequency of this resonance has not been calculated, it is excpected to be on the order of 100 cps or more, and would have a minor effect on the valve response.

5.2.4.2 Performance of the Uncompensated Temperature Control

The uncompensated system was subjected to a number of tests to demonstrate its response for varying gains and sampling frequency. One test was to determine the gain required for marginal stability as sampling frequency was varied. Test data is shown in Figure 5.2-32. All of the runs are parameterized by the control gain, which was set by potentiometer Q09. This pot setting can be transformed roughly into open-loop gain by multiplying by 80.

The stability criterion which was used in developing this data was established to cope with the nonlinear gains. Due to these gains (in the valves and lines), it is difficult for the system to produce oscillations which grow without bound, since increases in the pressure excursions cause a decrease in effective gains of the lines and valves. As a result, the system will go into limit cycles of increasing amplitude as the control gain is increased.

Figure 5.2-33 shows what might be considered "good" responses for various sampling rates. For each case, the gain is adjusted until reasonable results are obtained. The gains and sampling rates for each response are:

Response	Sampling Rate (samples/sec)	Gain Q09 Pot Setting
A	100	0.3
B	80	0.2
C	60	0.2
D	40	0.2
E	20	0.1
F	20	0.15

At the present time, a sampling rate of 40 samples/sec has been chosen because it produces reasonable results, and is compatible with present circuit designs. A sampling rate of 40 samples/sec and a gain on Q09 of 0.4 are used for design of the compensation. Figure 5.2-32 indicates that this will be an unstable condition for the uncompensated system. System response is shown in Figure 5.2-34. The response to a positive step in heat input is reasonably

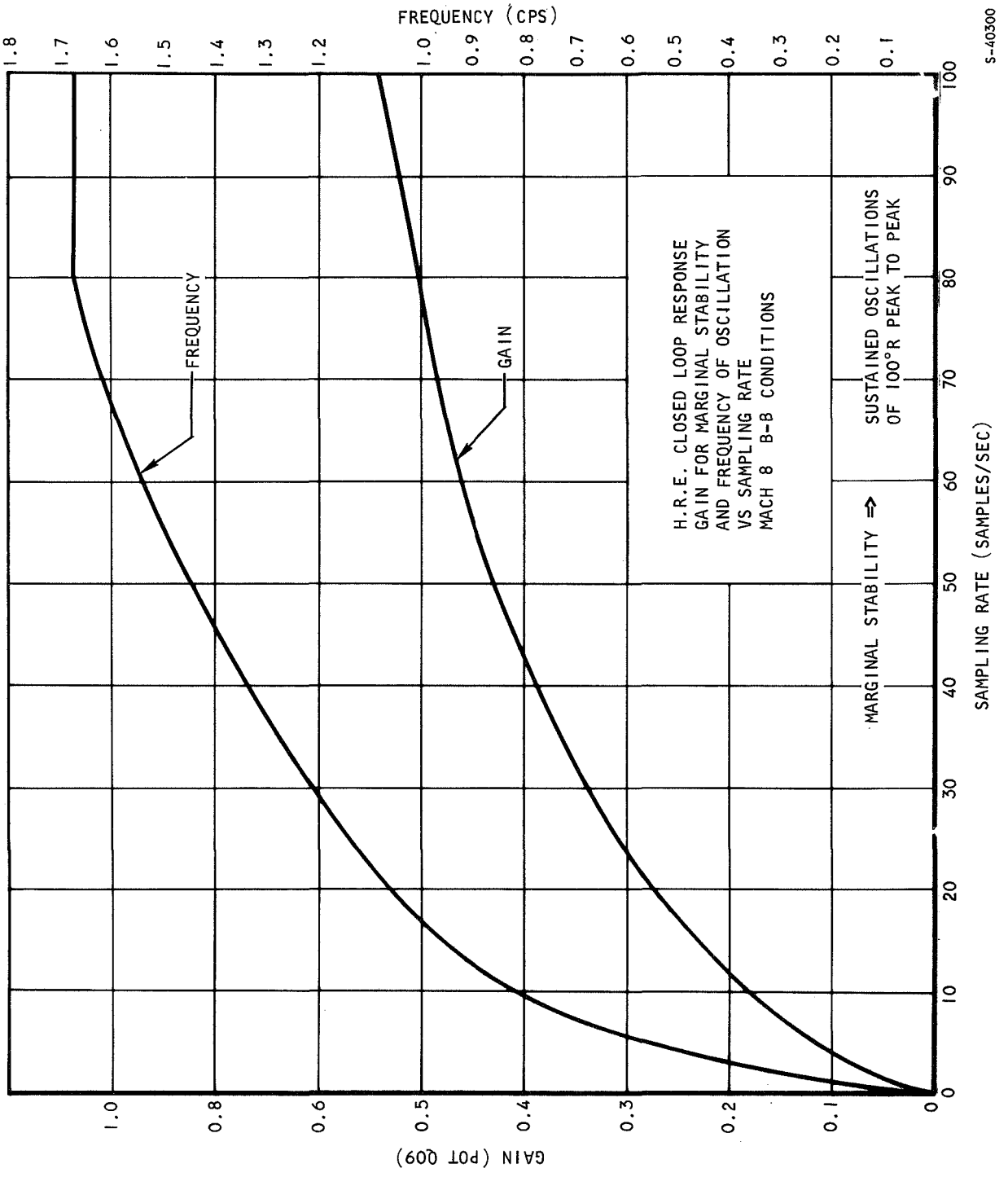

Figure 5.2-32 Gain for Marginal Stability.

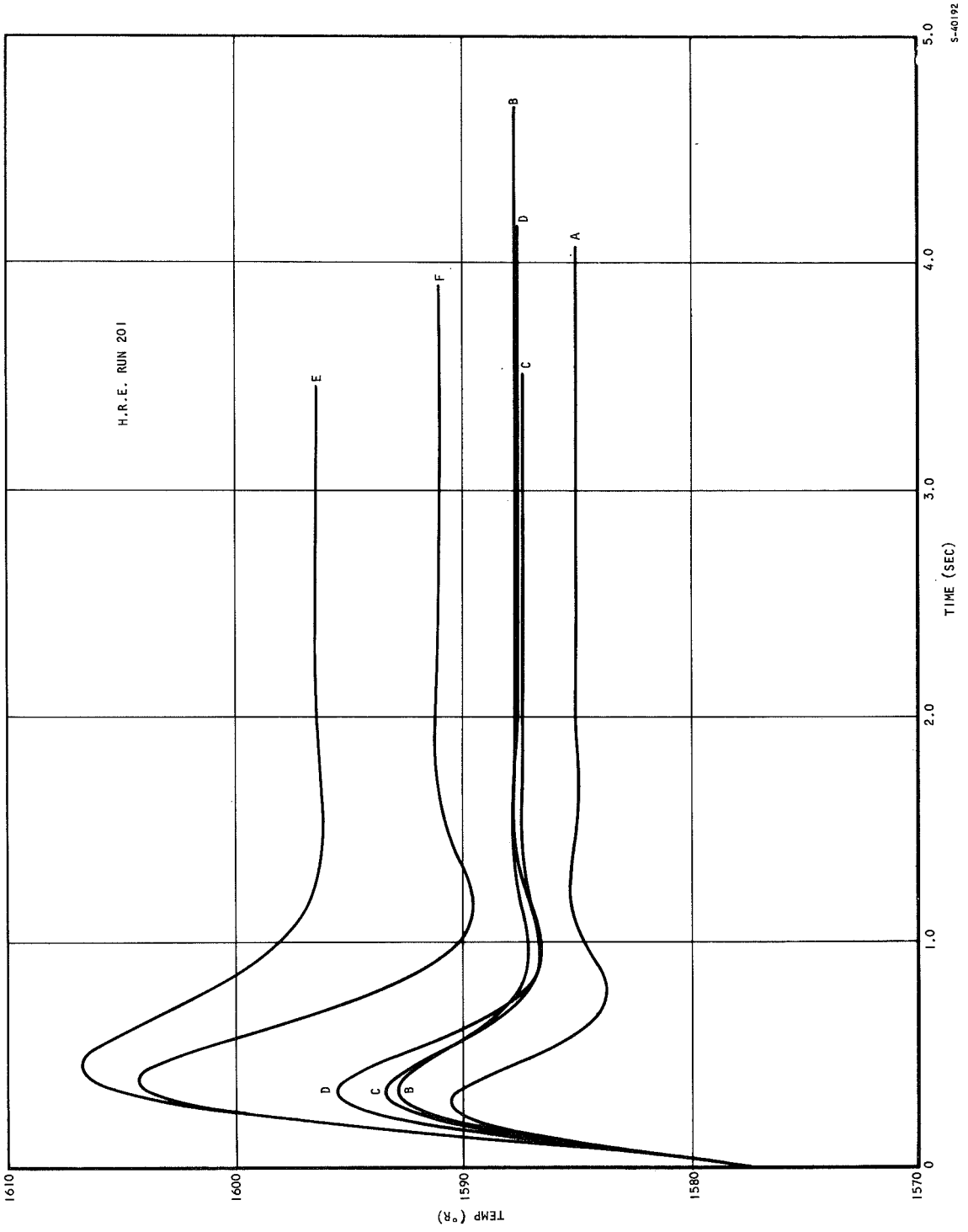

Figure 5.2-33 Response for Varying Sampling Rates and Gains.

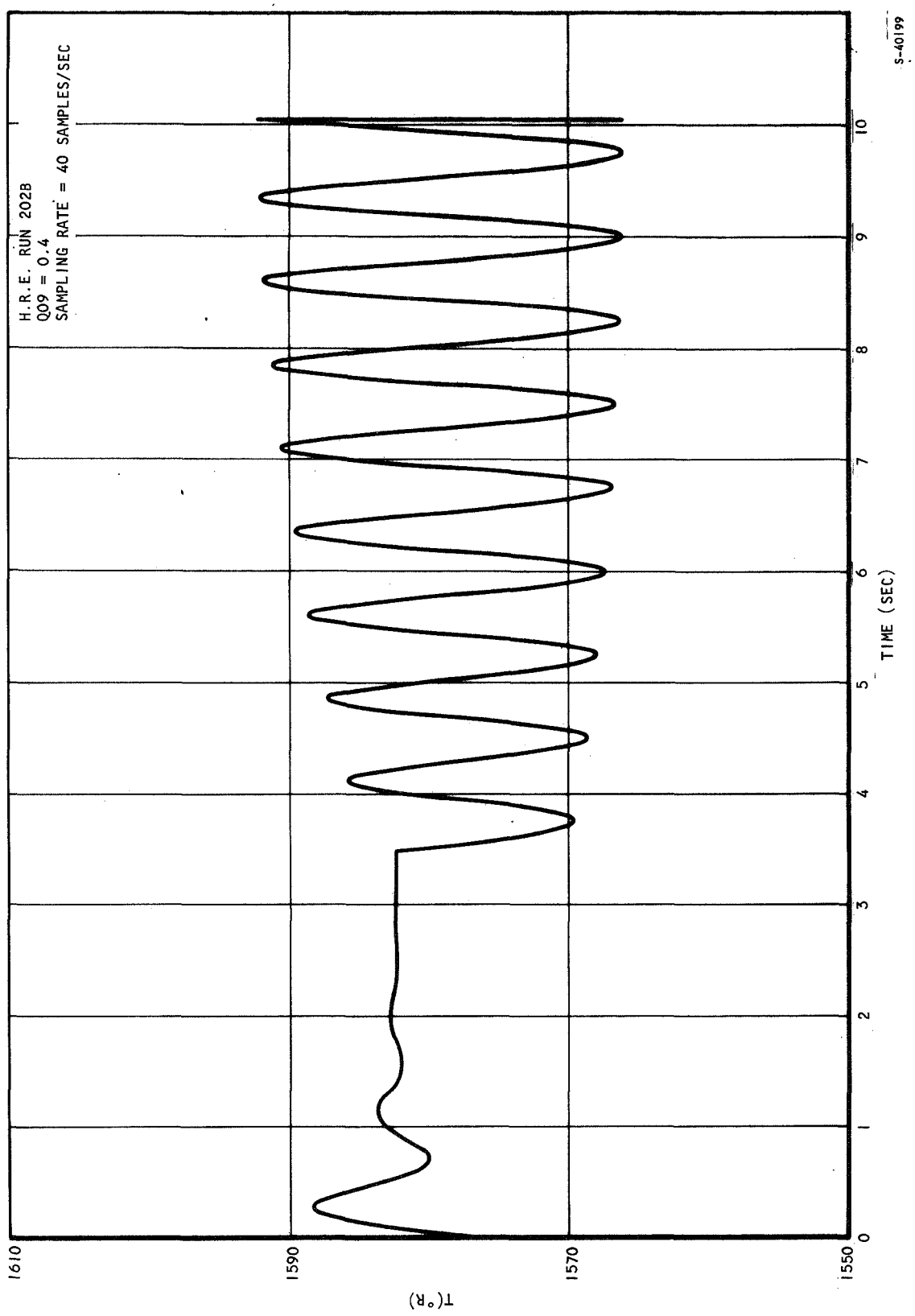

Figure 5.2-34 Response for Q09 = 0.4.

stable; removal of the step produces an unstable response due to the gain reduction which occurs with higher pressure levels.

5.2.3.3 Continuous Data Compensation

Both sampled data continuous data compensators were tested in the control. All compensators tested could be realized with relatively simple R-C network configurations.

The first compensation tried was a continuous data lead network, which had a transfer function of:

$$\frac{E_o}{E_i} = \left(\frac{St\alpha}{St\beta}\right)\left(\frac{\beta}{\alpha}\right)$$

where E_i = input voltage

E_o = output voltage

S = Laplace operator

Experimentation led to the "best" values of

$\alpha = 8$ (rad/sec)

$\beta = 80$ (rad/sec)

Figure 5.2-35 shows the response of temperature, valve area, flow through the valve, the track and store, and the compensation output to 10-percent steps in heat flow rate. The effect of the lead circuit is still go give valve area a "lead" over the output of the track and store. This simple lead circuit can stabilize the system response for gains of Q09 = 0.4.

A second-order lead circuit was then tested. Its transfer function was:

$$\frac{E_o}{E_i} = \frac{(St\alpha)}{(St\beta)}\frac{(St\gamma)}{(St\delta)}\left(\frac{\beta\delta}{\alpha\gamma}\right)$$

The values of α and β were set at 8 and 80, and then values of γ and δ were determined experimentally. The values chosen were:

$\gamma = 20$ (rad/sec)

$\delta = 40$ (rad/sec)

In testing this circuit, it was impossible to use a larger lead ratio (δ/γ) than 2 because several of the amplifiers would overload whenever 2 was exceeded. Figure 5.2-36 shows the system response for this case. The performance for the removal of the step in heat flow can be seen to be considerably improved. In all of these runs, it seems that valve flow, W_9, "leads" valve area. This

FIGURE 34. SYSTEM RESPONSES WITH 1ST ORDER LEAD CIRCUIT IN SERIES

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Figure 5.2-35. System Response with First-Order Lead Compensator

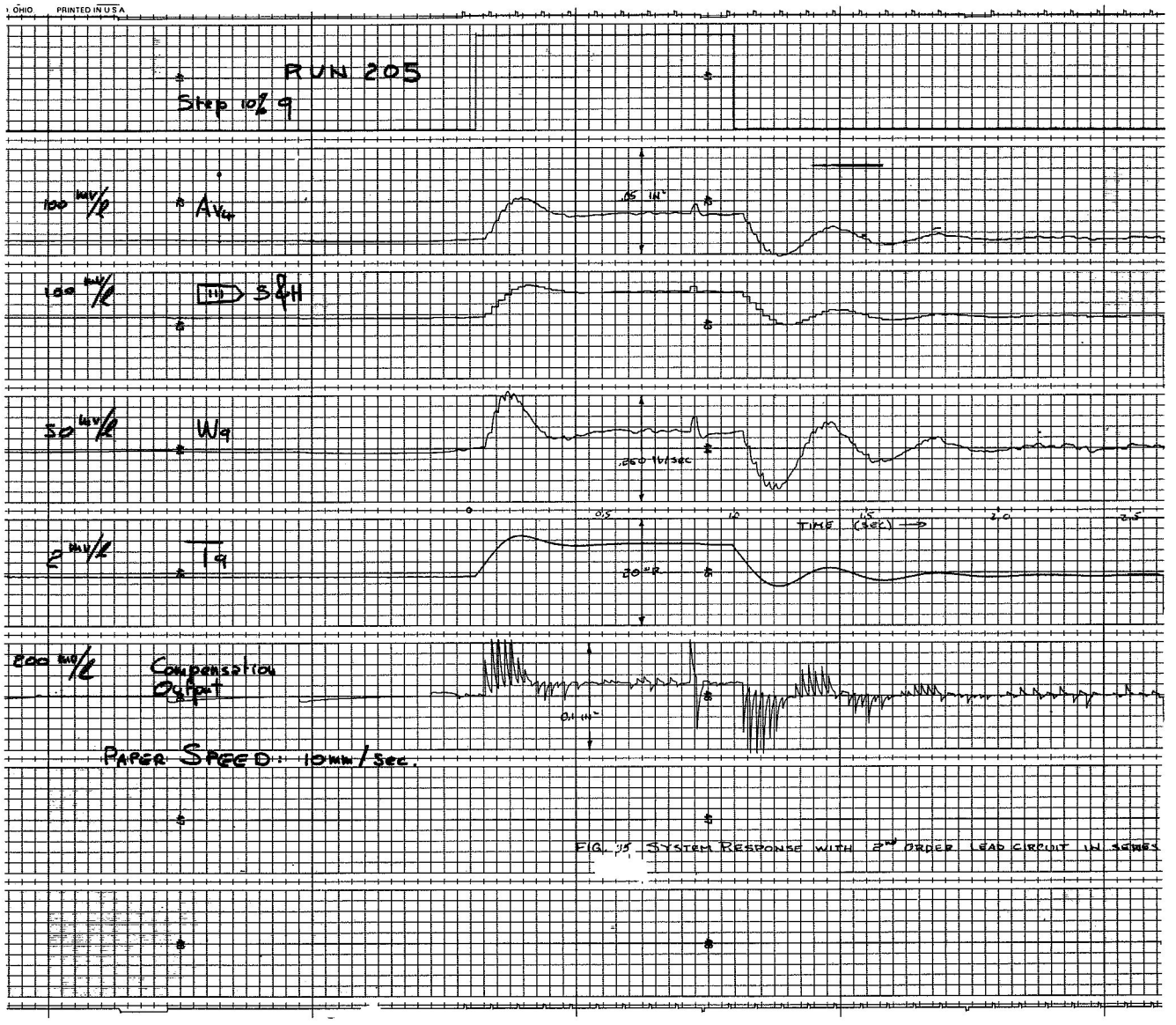

FIG. 15 - SYSTEM RESPONSE WITH 2ND ORDER LEAD CIRCUIT IN SERIES

S-40468

Figure 5.2-36. System Response with Second-Order Lead Compensator

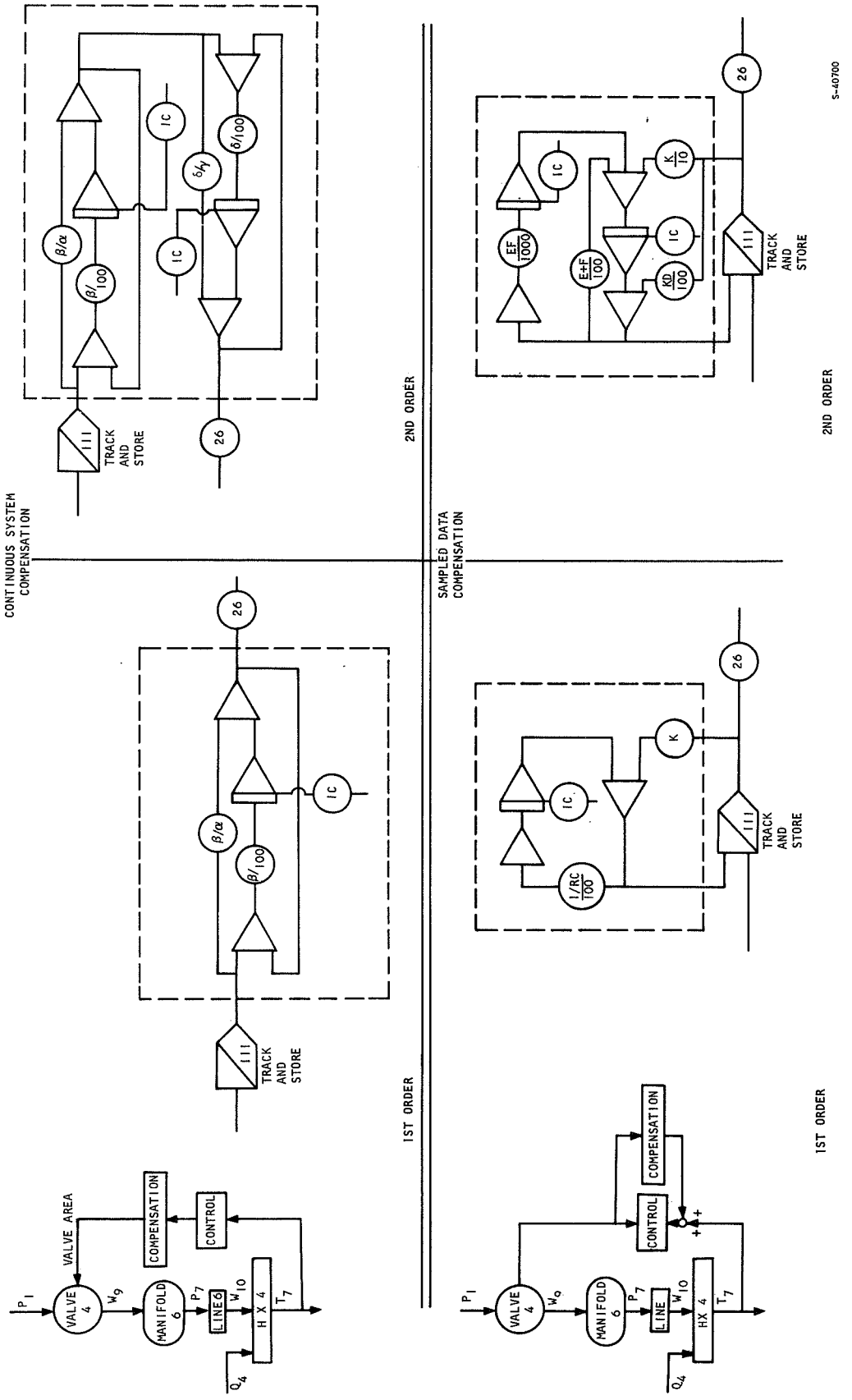

Figure 5.2-37. Compensation Circuits

is, in fact, the case, and this relationship has been established during the frequency response runs although not previously discussed. All of the compensation circuits are shown in Figure 5.2-37.

5.2.4.4 Digital Compensation

Digital compensation is distinct from continuous compensation in that its output changes only at the sampling instants. There are two ways that R-C networks can be used to produce digital compensation: they are shown in Figure 5.2-38.

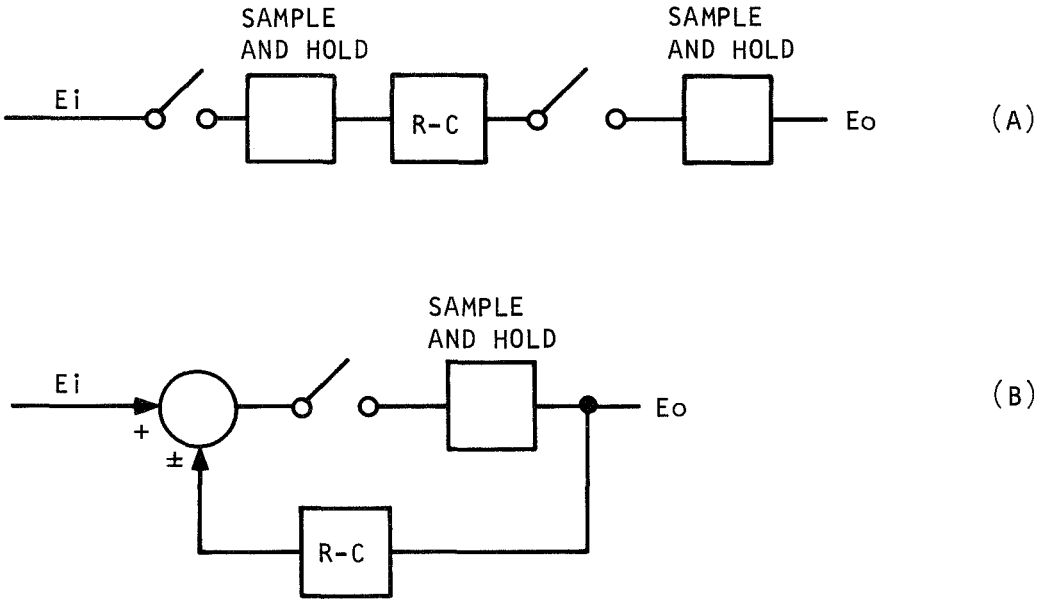

Figure 5.2-38. Digital Compensation Techniques

Method (B) was chosen, due to its savings of one sample and hold circuit, and due also to the relative ease with which the Laplace transform of the R-C network can be derived from the Z-transform of the compensator.

Experience in the "Interim Heat Exchanger Study" has shown that if rate compensation would improve the performance of the linear system, a digitally implemented rate compensation would improve the performance of the sampled data system. Since rate compensation cannot be realized by method (B), it was decided that the first digital compensator would be the digital equivalent

of the first-order lead circuit. The lead circuit had the following Laplace transfer function:

$$\frac{E_o}{E_i} = \left(\frac{S + \alpha}{S + \beta}\right)\left(\frac{\beta}{\alpha}\right)$$

or,

$$\alpha S E_o + \alpha\beta E_o = \beta S E_i + \alpha\beta E_i \qquad (5\text{-}33)$$

$$\frac{SE_o}{\beta} + E_o = \frac{SE_i}{\alpha} + E_i$$

Since the Laplace operator "S" implies differentiation with respect to time, equation (5-33) is equivalent to:

$$\frac{\dot{E}_o}{\beta} + E_o = \frac{\dot{E}_i}{\alpha} + E_i \qquad (5\text{-}34)$$

If β is made infinitely large, this will be equivalent to rate compensation. A decrease in α corresponds to an increase in rate feedback.

A digitally calculated rate signal would be

$$\dot{E} \rightarrow \frac{E(t) - E(t - T)}{T} \qquad (5\text{-}35)$$

where t = present time

T = sampling period

Since the operator Z^{-1} implies a time delay of one sampling period, the Z-transform of a digitally implemented rate signal would be:

$$\dot{E} \rightarrow \frac{E(Z) - Z^{-1}E(Z)}{T} = \frac{E(Z)}{T}(1 - Z^{-1}) \qquad (5\text{-}36)$$

Putting this information into equation (5-34), the Z-transfer function of a digitally implemented lead circuit is found:

$$E_o \frac{(1 - Z^{-1})}{\beta T} + E_o = E_i \frac{(1 - Z^{-1})}{\alpha T} + E_i$$

$$E_o\left(1 + \frac{1 - Z^{-1}}{\beta T}\right) = E_i\left(1 + \frac{1 - Z^{-1}}{\alpha T}\right)$$

$$\frac{E_o}{E_i} = \frac{1 + \frac{1 - Z^{-1}}{\alpha T}}{1 + \frac{1 - Z^{-1}}{\beta T}} = \frac{\beta}{\alpha} \frac{(\alpha T + 1 - Z^{-1})}{(\beta T + 1 - Z^{-1})}$$

$$= \frac{\beta}{\alpha} \frac{(1 + \alpha T)}{(1 + \beta T)} \left(\frac{Z - \frac{1}{1 + \alpha T}}{Z - \frac{1}{1 + \beta T}} \right)$$

In the Z-plane, this compensator will have a zero and a pole, whose locations are:

$$\text{zero at } \frac{1}{1 + \alpha T}$$

$$\text{pole at } \frac{1}{1 + \beta T}$$

As α gets smaller, which is equivalent to increasing the rate signal, the location of the Z-plane zero tends toward 1.0. As β is increased, the Z-plane pole moves toward the origin; this corresponds to making the lead compensator more like pure rate compensation.

The computations and programs which were used to implement the digital compensation are presented in Appendix C. This compensation could be realized by using an R-C circuit whose transfer function was

$$\frac{E_o}{E_i} = \frac{KS}{S + \frac{1}{RC}}$$

This circuit was put in the feedback loop of the track and store amplifier, using positive feedback. A digital computer program was written to relate K and 1/RC to α and β. The values which produced the best response were:

α = 9.0

β = 360.0

K = 0.7959

1/RC = 8.117

$$\frac{1}{1 + \alpha T} = \frac{40}{49} \cong 0.8$$

$$\frac{1}{1 + \beta T} = 0.1$$

NOTE: Since the sampling rate is 40 samples per second, T is 1/40 of a second

The value of α is very similar to the value of α chosen for the continuous lead compensation. System response is shown in Figure 5.2-39. This response is comparable to that which was achieved with the continuous first-order compensator.

The design of a second-order digital compensator started with a Z-transfer function:

$$\frac{E_o}{E_i} = \frac{(Z - \alpha)(Z - \gamma)}{(Z - \beta)(Z - \delta)} \quad \frac{(1 - \beta)(1 - \delta)}{(1 - \alpha)(1 - \gamma)}$$

Where the first-order compensation had one Z-plane zero and one pole, this has two zeros and two poles. Also, this compensation admits the possibility of locating the poles on the negative real axis of the Z-plane. The constant term is included to ensure that the steady-state gain of the device is one. The resulting transfer function of the feedback device was:

$$\frac{E_o}{E_i} = \frac{KS\ (S + D)}{(S + E)(S + F)}$$

The experimental approach was to fix α and β at the values which were established in the testing of the first order circuit (0.8 and 0.1, respectively), and find the best location for γ and δ. The locations of γ and δ were then fixed, and α and β were moved from their original locations, to find their new best locations. This process would possibly have profited from further iterations, but the time required for the iterations was prohibitive. The final values were

$\alpha = 0.7$

$\beta = 0.4$

$\gamma = 0.65$

$\delta = -0.8$

$K = 0.9583$

$D = 28.4$

$E = 16.89$

$F = 14.11$

System response is shown in Figure 5.2-40. The temperature responses are shown in Figures 5.2-41 through 5.2-44. A summary of the performance characteristics for a gain of Q09 = 0.4 and a 10-percent step reduction in heat flow is shown in Figure 5.2-45. All systems had the same rise time, 0.1 sec. The response of the digitally compensated system for varying values of the gain

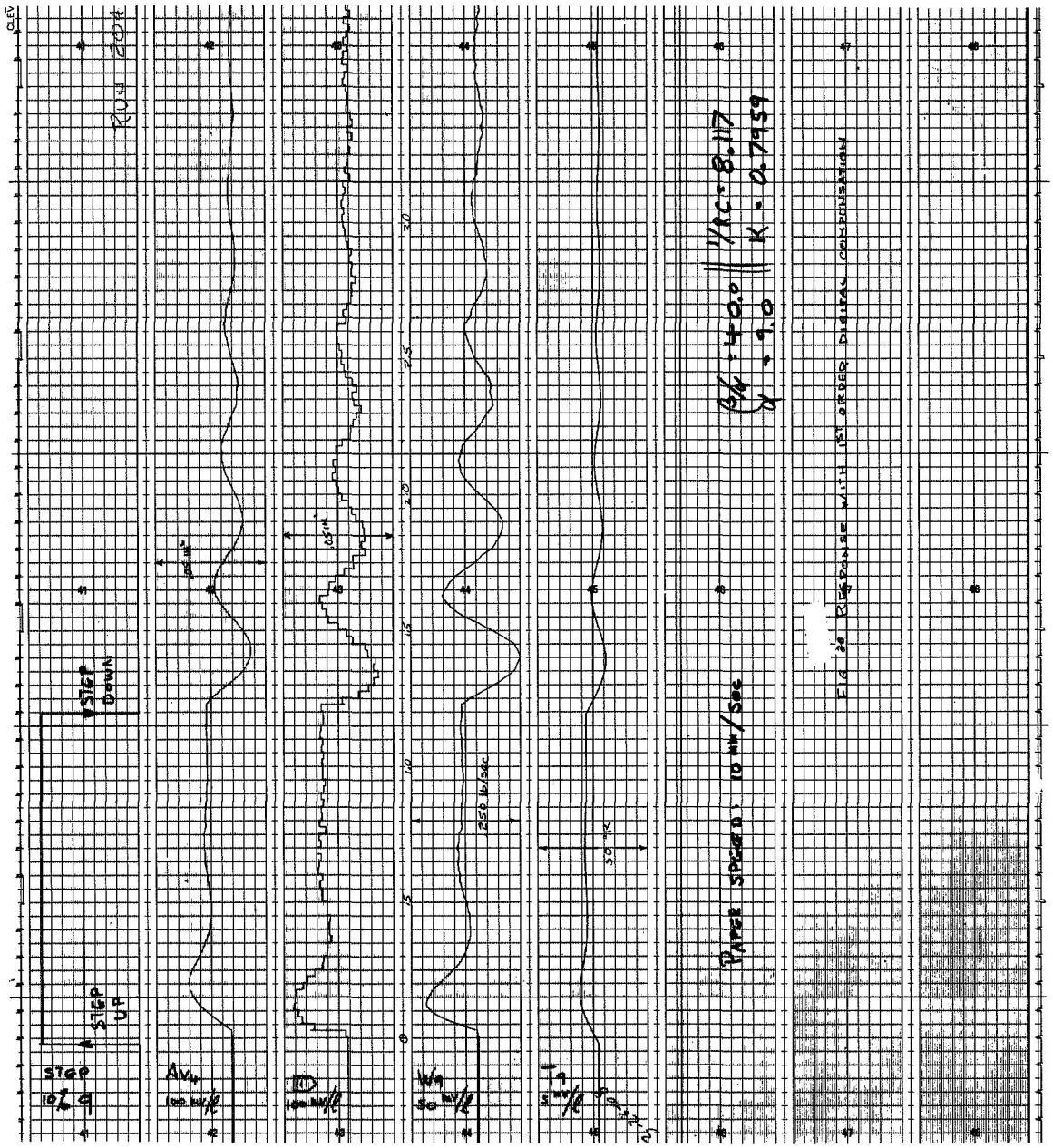

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Figure 5.2-39. System Response with First-Order Digital Compensation

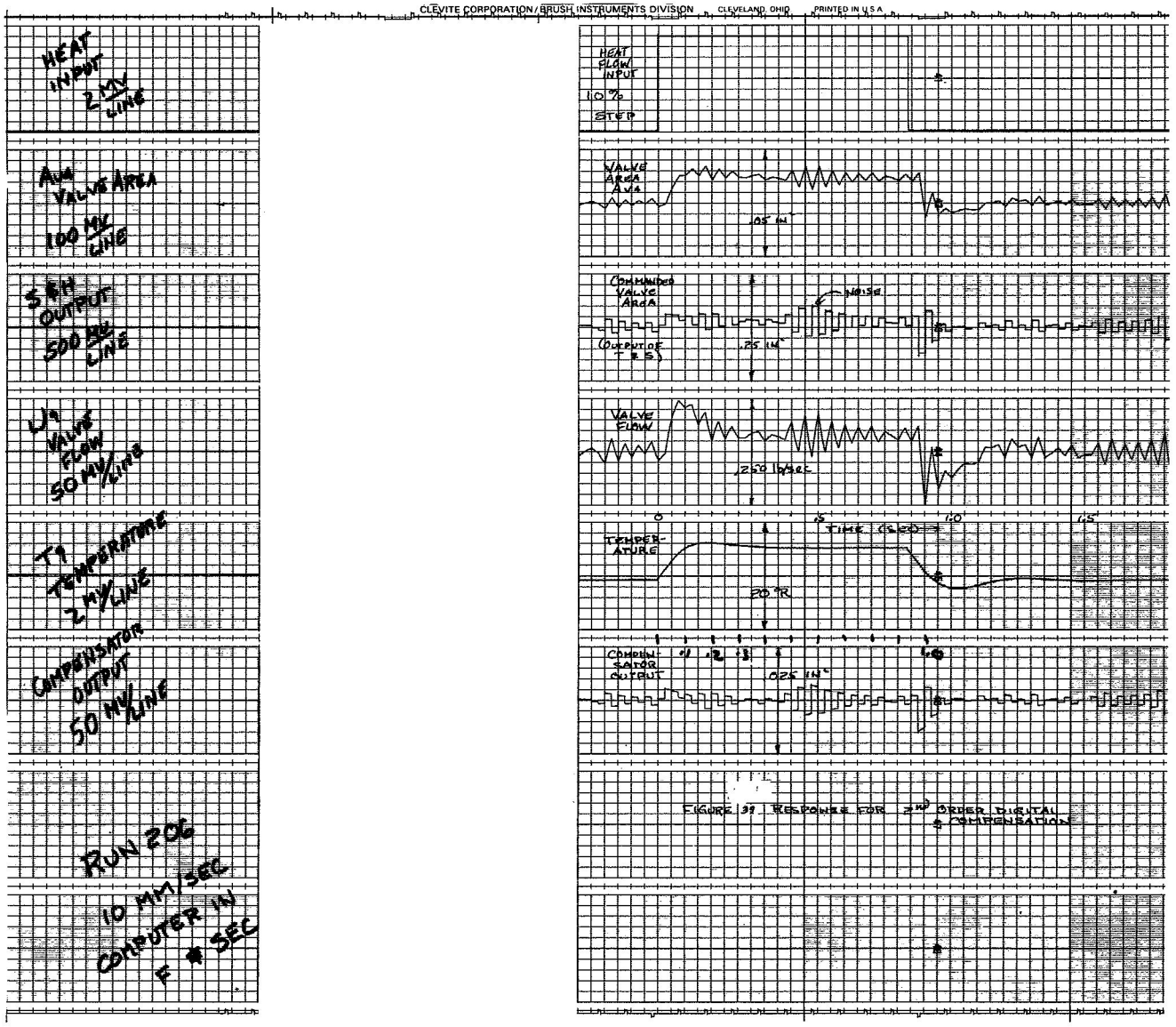

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Figure 5.2-40. System Response with Second-Order Digital Compensation

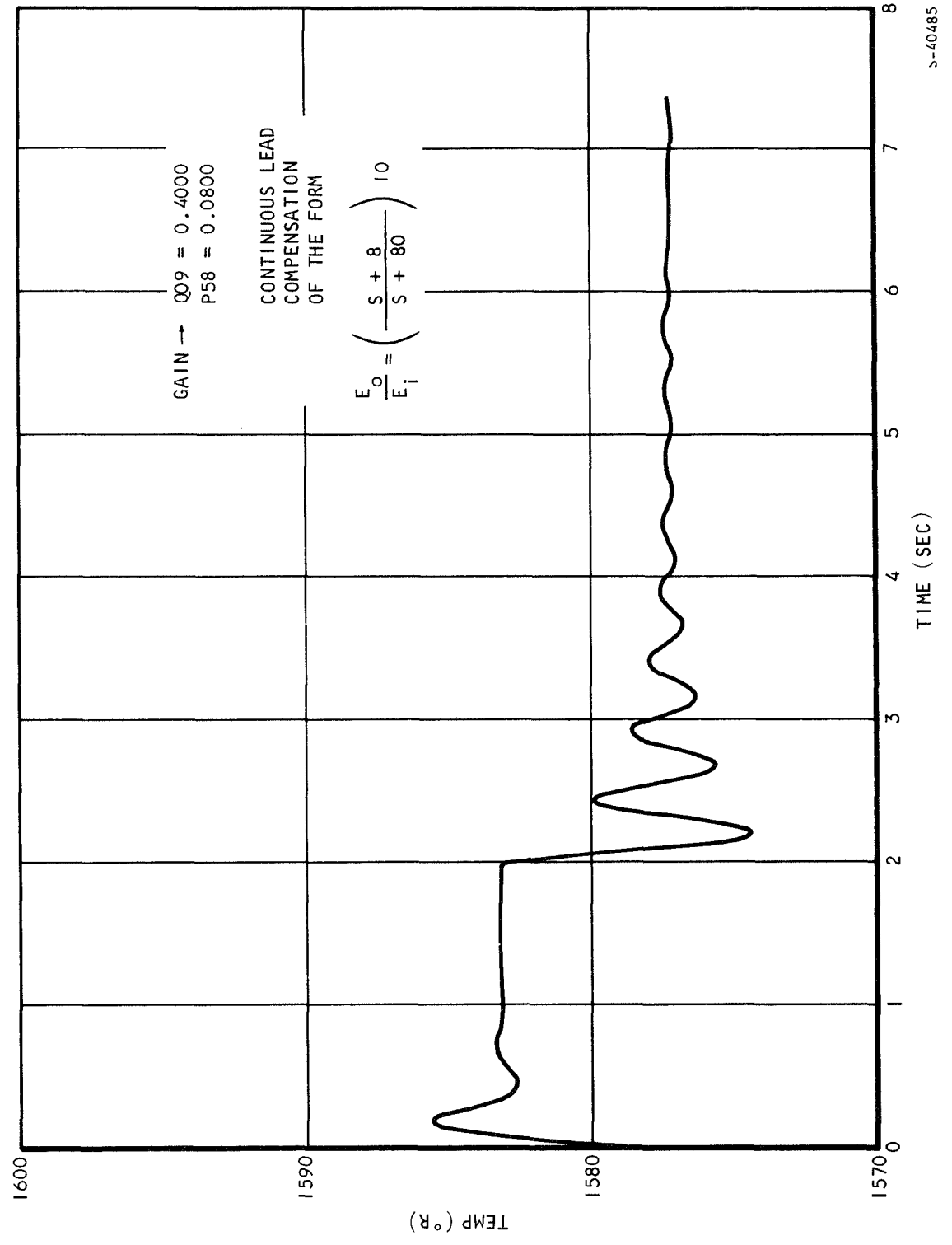


Figure 5.2-41. Run 203

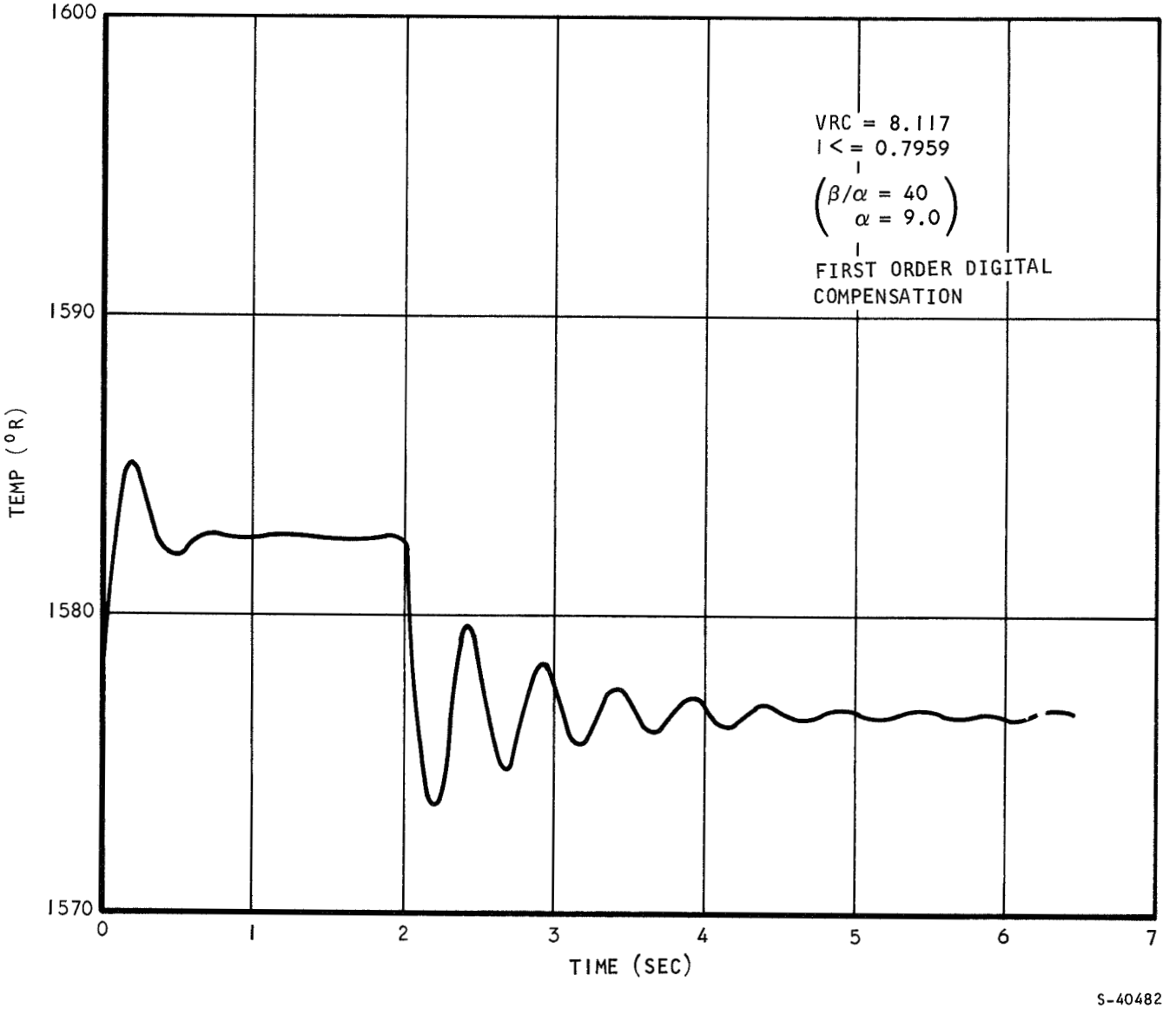


Figure 5.2-42. Run 204

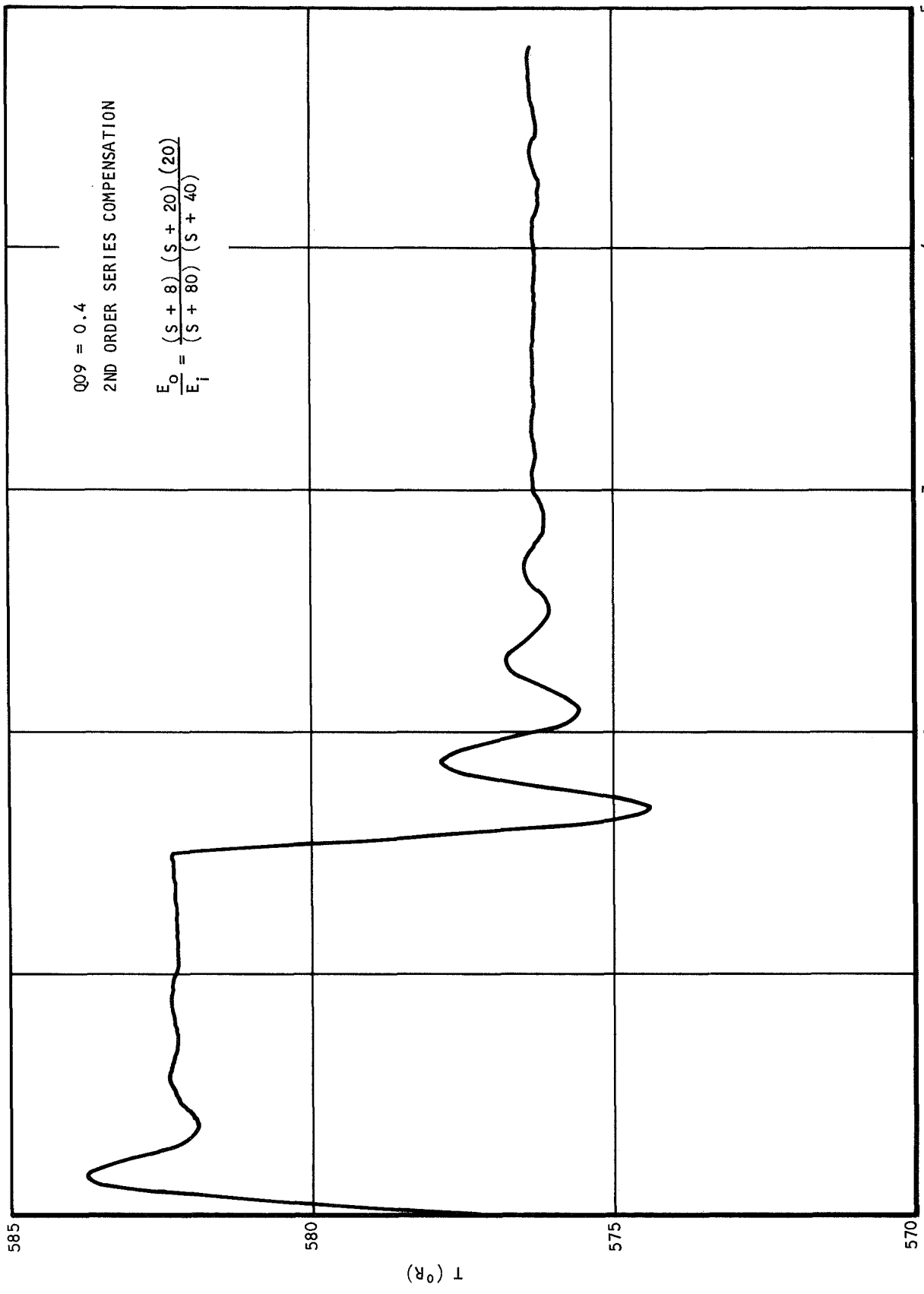


Figure 5.2-43. Run 205

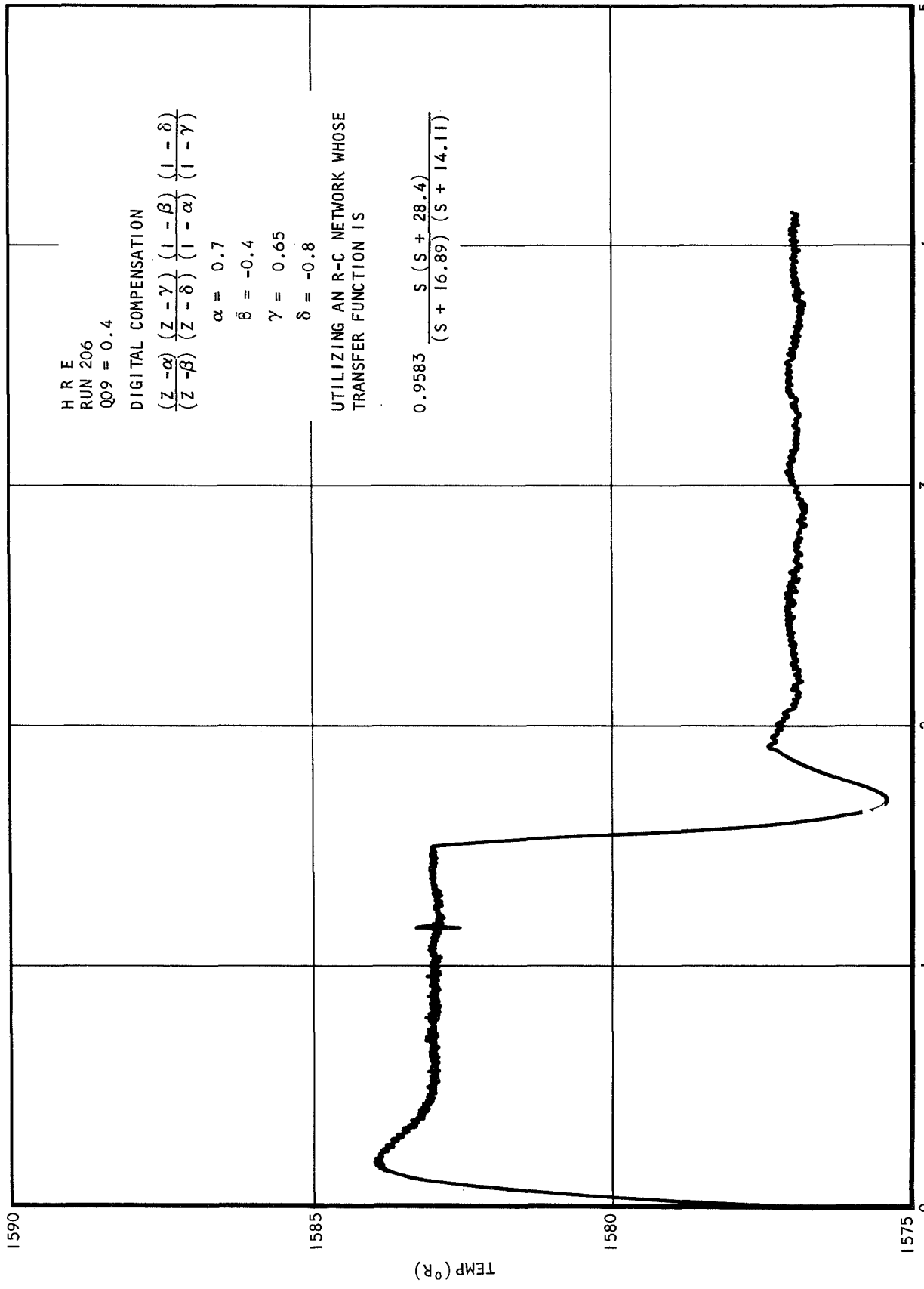


Figure 5.2-44. Run 206

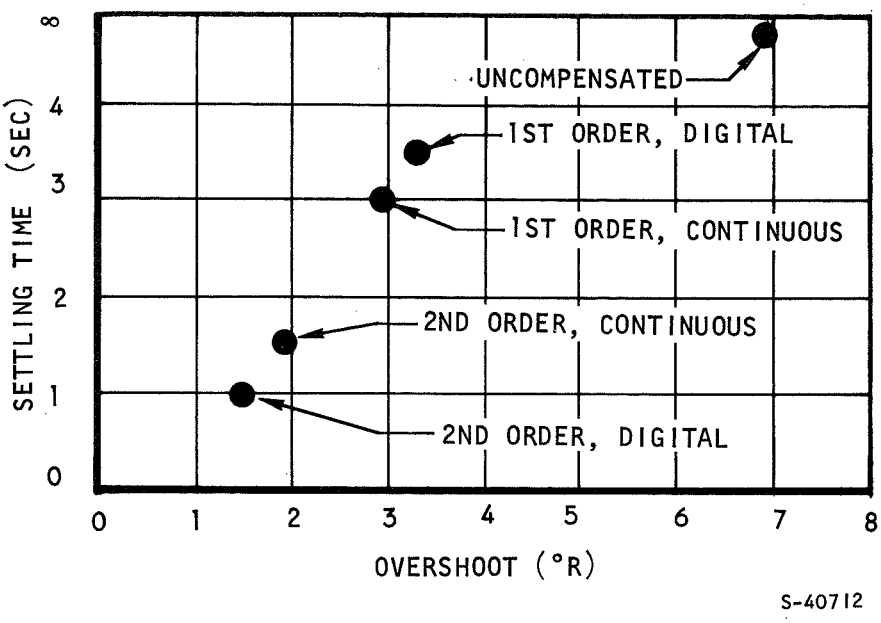


Figure 5.2-45. Summary of Performance

potentiometer Q09, are shown in Figures 5.2-46 through 5.2-48. The system becomes marginally stable for a gain of 1.1, with a frequency of about 4.2 Hz. The use of compensation in this case has increased the gain for marginal stability by a factor of 3.

5.2.3.5 Design Information

The design information which was sought concerned the gains of the various temperature controls, the compensation to be used, and the values of the control temperatures. Assumptions made were: (1) that the system will be capable of performing with gains as high as implied by having potentiometer Q09 equal to 1.1 (or an open-loop gain of about 90); (2) that the digital compensation configuration would be the same as in the simulator; and (3) that the minimum valve area will be 0.05 sq in.

Calculations central to the determination of control gain and control temperature were (1) determination of the open-loop gain which corresponds to a given value of potentiometer Q09, and (2) an estimate of how much the gain of the system can be expected to vary.

A rough schematic of the system is shown in Figure 5.2-49. The gain of the valve driver is equal to one in the simulation. The open-lip gain is

$$K = K_1 K_2$$

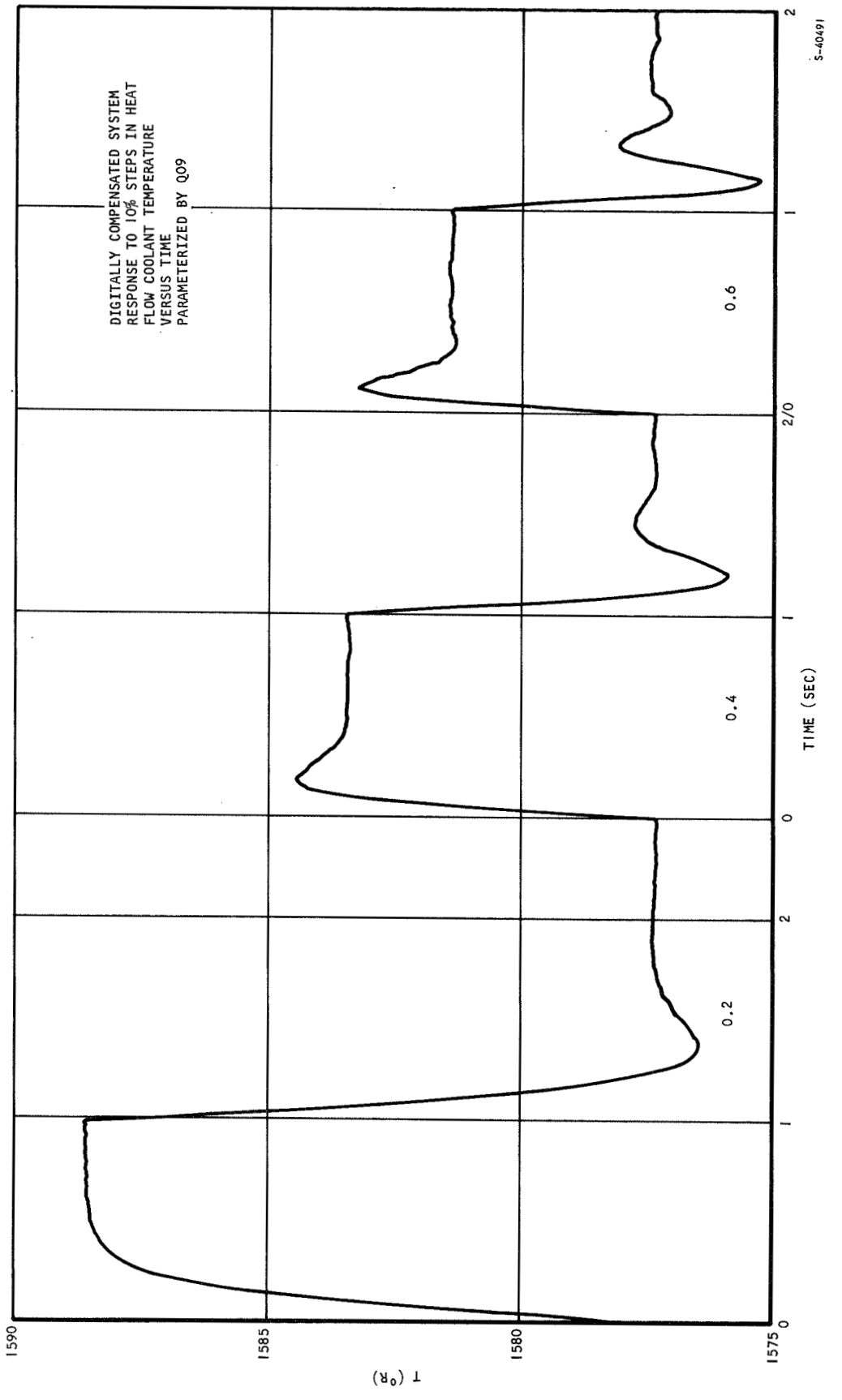


Figure 5.2-46. Run 207A

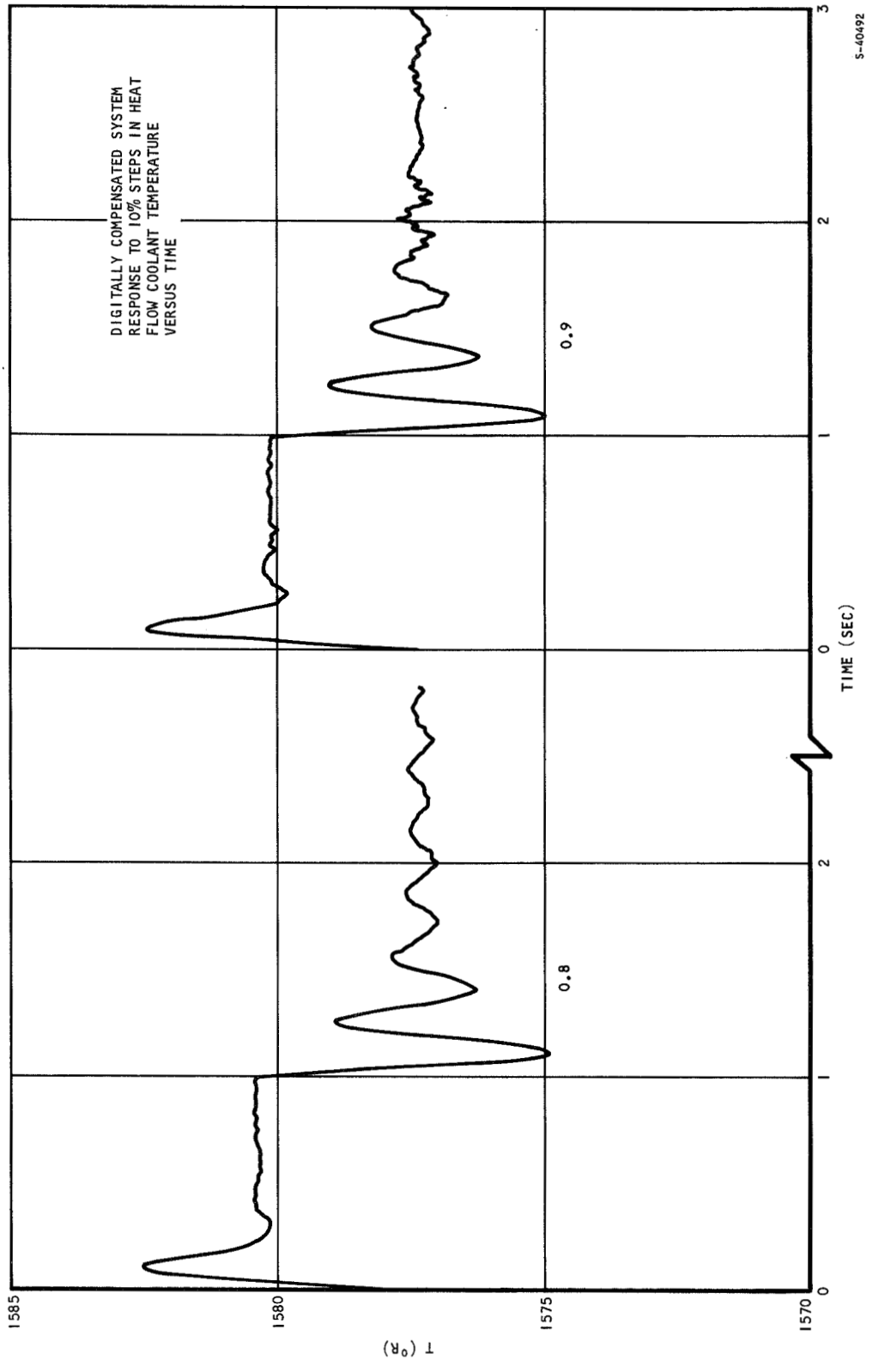


Figure 5.2-47. Run 207B

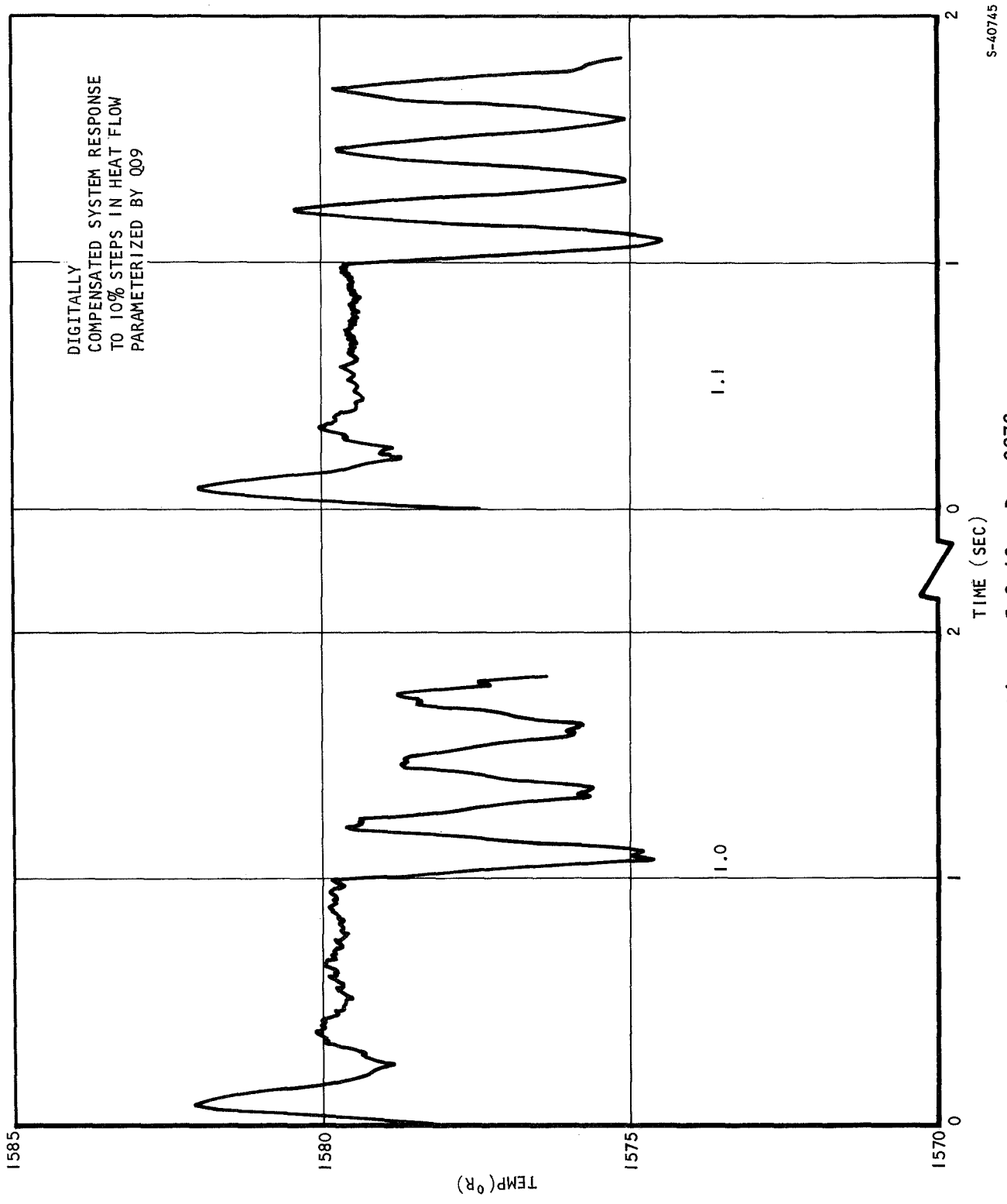
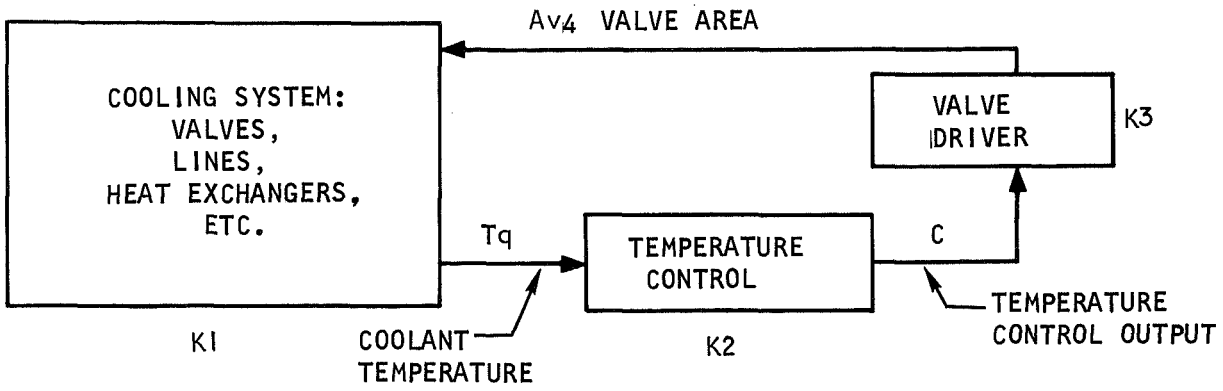


Figure 5.2-48. Run 207C



$$K1 = \frac{\partial Tq}{\partial Av4}$$

$$K2 = \frac{\partial C}{\partial Tq}$$

$$K3 = \frac{\partial Av4}{\partial C}$$

S-40740

Figure 5.2-49. System Schematic

K_2 may be calculated from knowledge of the value of potentiometer Q09. The value of the scaled gain, K_2^*, is given by

$$K_2^* = Q09 \times 100 = \frac{\partial Av^*}{\partial T_9^*} = \frac{\partial\left(\frac{Av4}{AvMax}\right)}{\partial\left(\frac{T_9}{T_{MAX}}\right)}$$

$$K_2^* = \frac{\partial Av4}{\partial T} \cdot \frac{T_{Max}}{Av_{Max}} = K_2 \cdot \frac{T_{Max}}{Av_{Max}}$$

$$K_2 = Q09 \times 100 \times \frac{Av_{Max}}{T_{Max}} \qquad Av_{Max} = 0.1 \text{ in.}^2 \qquad T_{Max} = 2000^{\circ}R$$

$$K_2 = Q09 \times \frac{100 \times 0.1}{2000} = Q09 \times 5 \times 10^{-} \quad \frac{\text{in.}^2}{^{\circ}R}$$

A static test of the system was made to determine K_1. Only the area of valve 4 was changed, and steady-state temperature were recorded. This graph is shown in Figure 5.2-50. From it, the value of K_1 is shown to be about $1.65 \times 10^{4}{}^{\circ}R/\text{in.}^2$. Calculating the open-loop gain,

$$K = K_1 K_2 = 1.65 \times Q09 \times 5 \times 10 = 82.5\ Q09$$

The largest value of steady-state gain will be

$$Q09 = 1.1$$

$$K_{max} = 1.1 \times 82.5 = \underline{\underline{90.75}}$$

A simplified model of the system is constructed to estimate the amount of variation which will occur in the system gain, K_1 (Figure 5.2-51). To simplify the calculations, P_1 and P_9 are assumed to be constant. The equations which describe the device are:

$$W = \frac{C_2 P_1 AvN}{\sqrt{T_1}}$$

where W = flow, lb/sec

P_1 = upstream pressure, psi

Av = valve area, in.^2

N = function

T_1 = upstream temperature, $^{\circ}R$

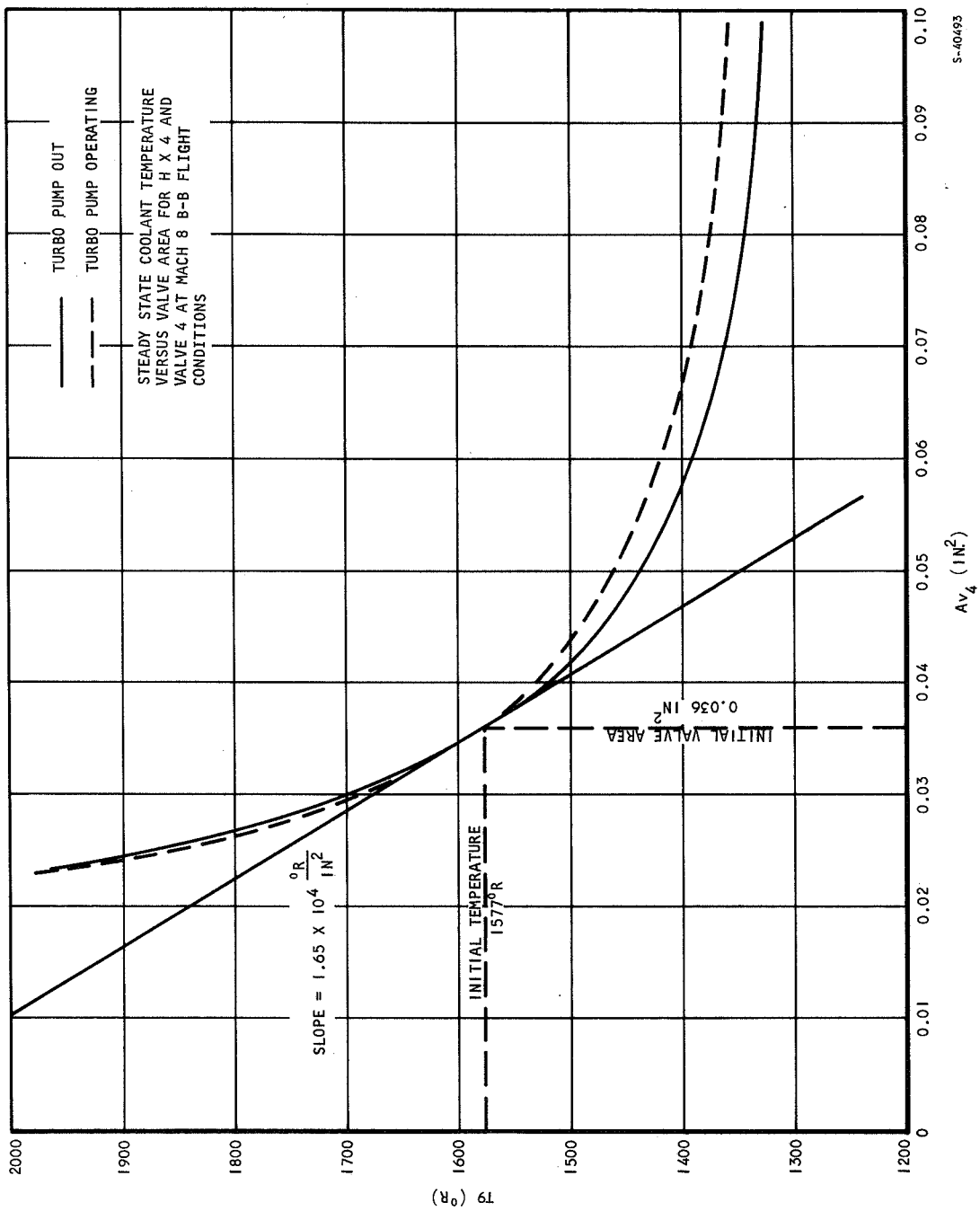


Figure 5.2-50. Steady-State Temperature vs Valve Area

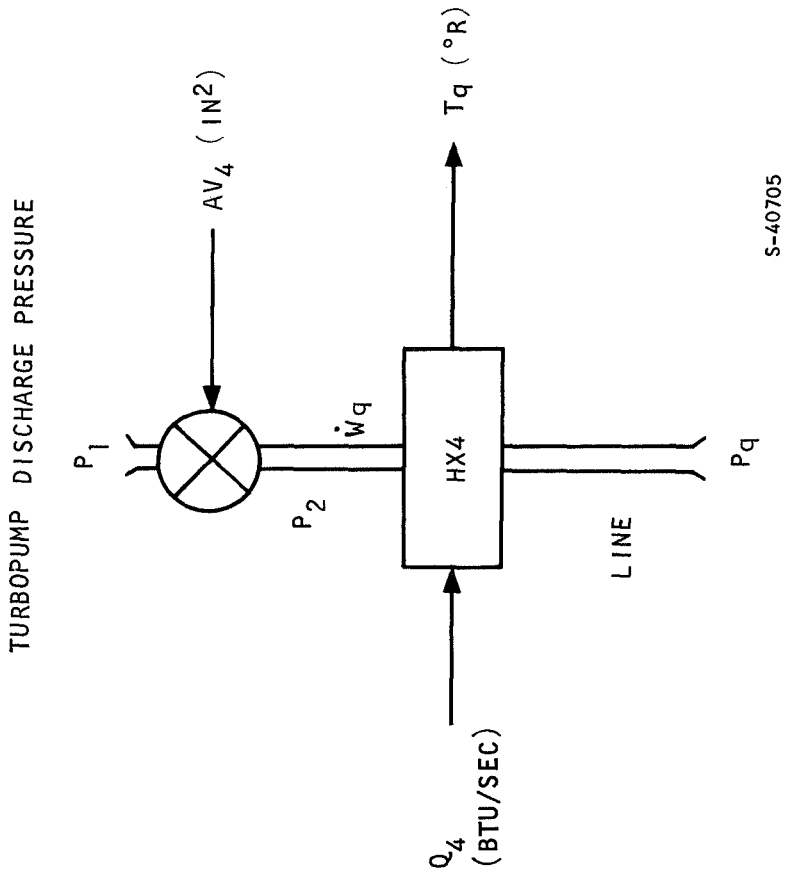


Figure 5.2-51. Simplified System

Line

$$\dot{W} = K\sqrt{P_7^2 - P_9^2}$$

Heat exchanger

$$\Delta T = \frac{Q}{\dot{W} C_p}$$

where K = line constant (in.^{2}/lb)

ΔT = temperature rise ($^\circ$R)

Q = heat flow input (Btu/sec)

C_p = specific

= 3.6 Btu/lb-$^\circ$R

The value of K_1 for this system may be found from:

$$K_1 = \frac{\partial T_9}{\partial Av4} = \frac{\frac{\partial \dot{W}}{\partial P_7} \cdot \frac{\partial T_9}{\partial \dot{W}}}{\frac{\partial Av}{\partial P_7}}$$

Equating flow through the valve and flow through the line,

$$\frac{C_2 P_1 Av N}{\sqrt{T_1}} = K\sqrt{P_7^2 - P_9^2}$$

$$Av = \frac{\sqrt{T_1}}{C_2 P_1 N} K\sqrt{P_7^2 - P_9^2}$$

$$\frac{\partial Av}{\partial P_7} = \frac{\sqrt{T_1}\, K}{C_2 P_1}\left\{ -\frac{\sqrt{P_7^2 - P_9^2}}{N^2}\frac{\partial N}{\partial P_7} + \frac{P_7}{\sqrt{N\,P_7^2 - P_9^2}} \right\}$$

$$= \left(\frac{\sqrt{T_1}}{C_2 P_1 N}\right)\left(K\sqrt{P_7^2 - P_9^2}\right)\left\{\frac{P_7}{P_7^2 - P_9^2} - \frac{1}{N}\frac{\partial N}{\partial P_7}\right\}$$

$$= \frac{Av4}{\dot{W}} \cdot \dot{W}\left\{\frac{1}{P_7\left(\frac{1 - P_9^2}{P_7^2}\right)} - \frac{1}{N}\frac{\partial N}{\partial P_7}\right\}$$

$$= Av4 \left\{ \frac{1}{P_7 \left(1-\left(\frac{P_9}{P_7}\right)^2\right)} - \frac{1}{N} \frac{\partial N}{\partial P_7} \right\}$$

The other partial derivatives are:

$$\frac{\partial \dot{W}}{\partial P_7} = \frac{K P_7}{\sqrt{P_7^2 - P_9^2}} = \frac{\dot{W}}{P_7 \left(1-\left(\frac{P_9}{P_7}\right)^2\right)}$$

$$\frac{\partial T_9}{\partial \dot{W}} = \frac{Q}{\dot{W}^2 C_p} = - \frac{\Delta T}{\dot{W}}$$

The steady-state gain is:

$$K_1 = \frac{\frac{\dot{W}}{P_7 \left(1-\left(\frac{P_9}{P_7}\right)^2\right)} \cdot \frac{\Delta T}{\dot{W}}}{Av4 \left\{ \frac{1}{P_7 \left(1-\frac{P_9}{P_7}\right)^2} - \frac{1}{N} \frac{\partial N}{\partial P_7} \right\}}$$

$$= \frac{-\Delta T}{Av4 \left\{ \left(1 - \frac{P_7 \left(1-\left(\frac{P_9}{P_7}\right)^2\right)}{N}\right) \frac{\partial N}{\partial P_7} \right\}}$$

For our case,

P_1 = 1100 psi

P_7 = 946 psi

P_9 = 500 psi

$$Q_4 = 2240 \text{ Btu/sec}$$

$$Av4 = 0.036 \text{ in.}^2$$

$$N = 0.732$$

$$\frac{\partial N}{\partial P_7} = -1.94 \times 10^{-3} (\text{psi})^{-1}$$

$$\Delta T = 1477 \ ^{\circ}R$$

The calculated value is:

$$K_1 = 1.46 \times 10^4 \ ^{\circ}R/\text{in.}^2$$

The difference between the calculated value and the empirical value is due to the constant pressure assumption for P_1 and P_9 in the simplified model. The equation for K_1 can be put in the form:

$$K_1 = \frac{-\Delta T}{Av\ D}$$

where the value of D can be near 1, for low flows, or as high as 5, for high flows. In the gain calculations, a value of D of 2.0 was used, although the validity of this number cannot be established. The value of ΔT and the minimum value area are:

$$\Delta T_{max} = 1500$$

$$Av_{min} = 0.05$$

$$K_{1max} = -\frac{1500}{0.1} = -1.5 \times 10^4 \ \frac{^{\circ}R}{\text{in.}^2}$$

The open-loop gain of the actual system will be

$$K = K_1 K_2 K_3$$

If the maximum allowable value of K is 90, then the maximum allowable value of K_2K_3 is given by:

$$\frac{K_{Max}}{K_{1Max}} = \frac{90}{1.5 \times 10^4 \ \frac{^{\circ}R}{in^2}} = K_2K_3 \text{ Max} = 6 \times 10^{-3} \ \frac{\text{in.}^2}{^{\circ}R}$$

Since the maximum value of K_3 is known to be about 1.5 $\frac{\text{in.}^2}{\text{amp}}$, the value of K_1, the gain of the temperature control, is fixed.

$$K_2 = \frac{2 \times 10^{-3}}{1.5} \quad \frac{\text{in.}^2}{^\circ\text{R}} \frac{\text{amp}}{\text{in.}^2}$$

$$= 4 \text{ MA}/^\circ\text{R}$$

This gain is expected to be accurate to within a factor of 4.

The lowest expected open-loop gain can now be estimated, since the maximum value area is known to be 0.37 in.^3.

$$K_{1\min} = \frac{1500}{0.37 \times 2} = 2.40 \frac{^\circ\text{R}}{\text{in.}^2}$$

$$K_{\min} = 2140 \times 6 \times 10^{-3} = 12.84$$

If the temperature rise across a heat exchanger is 1500°R, then the standoff error in the temperature control will be:

$$T_{\text{error}} = \frac{\Delta T}{1 + K} T_{\text{max error}} = \frac{1500}{1.384} = \underline{\underline{109^\circ\text{R}}}$$

The control temperature, which is used to produce an error in the temperature control, must be about 100°R less than the maximum allowable temperature of 1600°R, or about 1500°. This figure is expected to be accurate to within 10 percent.

In addition to producing design information, this study also illustrates the extremely large gain variations that occur. With a control temperature of 1500°R and an open-loop gain of 90, the system steady-state error will be about 15°, and the temperature will therefore be controlled to about 1515°R rather than to the desired 1600°R. Subsequent overcooling will cause a certain amount of fuel waste. Since the control temperature is based on the minimum open-loop gain, this gain should be as high as possible.

This characteristic implies that the temperature control should be operated with the highest practical open-loop gains to permit a large minimum open-loop gain. Conditions such as low flow and small valve areas vs high flow and large valve areas are the underlying causes of the large gain spread. These conditions determine the worst-case droop as indicated above.

6.0 DESIGN EFFORT

6.1 DIGITAL COMPUTER

The computer is now in-house and is being used by engineers and programmers. Detailed programming continues as planned in the previous report. General characteristics and processor operation are detailed in Appendix D, to aid in comprehension of the computer operation and engine control programs.

6.1.1 Computer Operation

The computer and ground support equipment were delivered to AiResearch on January 31, 1968. The equipment operated properly except for a nixie tube in the display register and an intermittent flat pack associated with the control logic for the teletypewriter; both items are in the computer control console. After the defective parts were replaced, the acceptance test conducted at the manufacturer's facility was repeated for both the computer and the ground control equipment at room ambient only.

An hour-meter was permanently installed on the computer control console to record the time that power is applied to the computer control console. To date, 134 hr has been logged for the hardware system. The system has been used by engineers and programmers becoming familiar with the equipment prior to coupling the computer and the input/output control unit. No failures have occurred in either the computer or the control console.

6.1.2 Software Development

A major portion of the engine control system programs have been written but they remain to be assembled and tested on either the computer itself or on a software simulator.

The purpose of the assembly program is to convert the programming language from the convenient coding form (symobolic language) to a form, which may be loaded into the Micro D computer (Figure 6.1-1). The program is also compiled in a form suitable for input to an Interpretive Computer Simulation Program. This interpretive program faithfully reproduces the operation of a Micro D computer and, in addition, contains input/output simulators and numerous programming aids.

The coding language which the "assembler" accepts consists of instructions made up of three-letter operation abbreviations (Figure D-2, Appendix D) and multicharacter storage references.

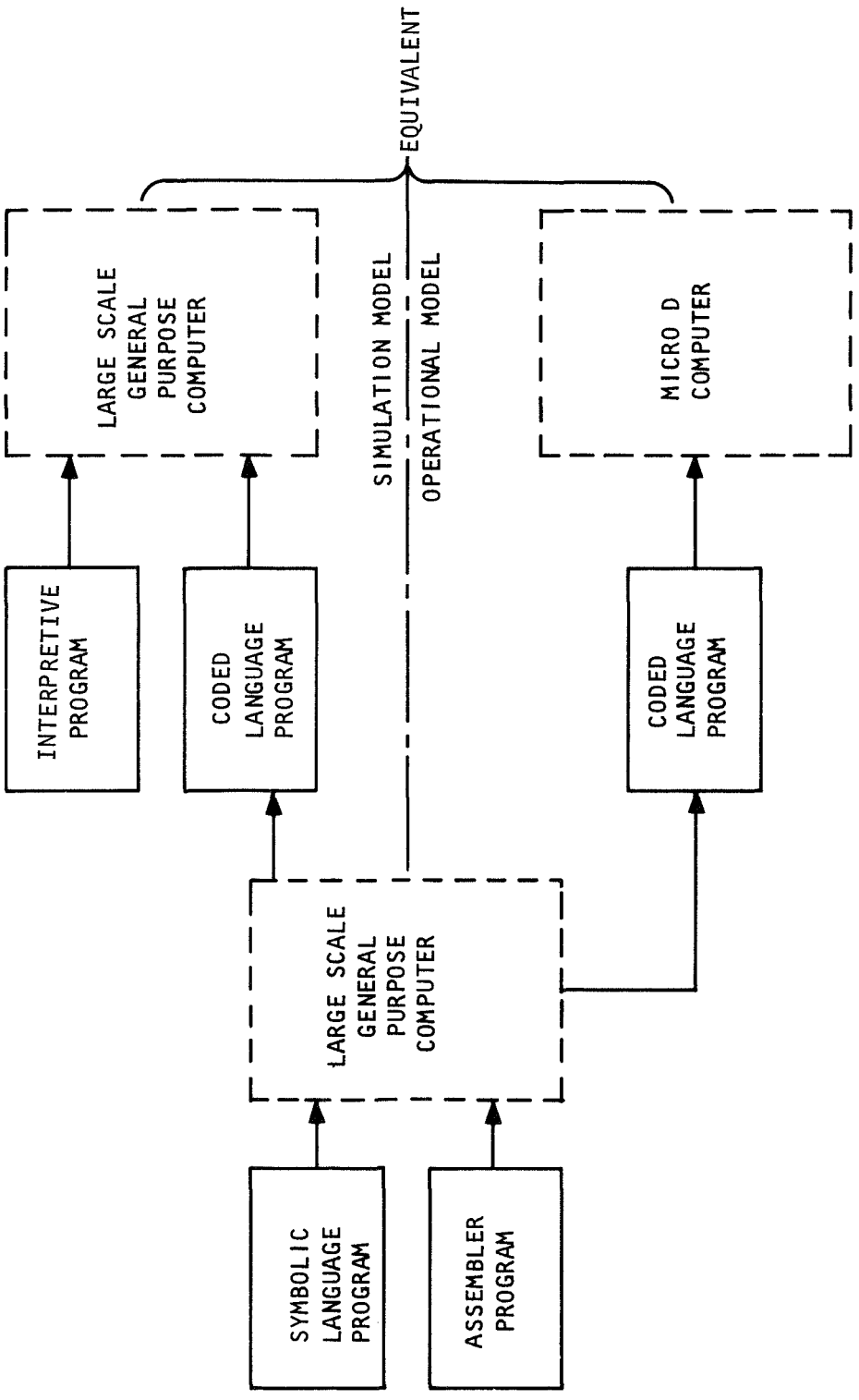


Figure 6.1-1. Program Assembly Procedure

The instructions are punched on 80-column IBM cards, one per card, and read onto magnetic tape; the tape is then used as an input to the assembly program.

The assembly procedure is divided into two parts. First, the assembler examines the particular program to be assembled (usually referred to as the source program) and assigns binary numbers to each symbol used in writing the program. Second, the assembler, using the symbol table formed in the previous step, prepares the actual machine language program and stores it in a convenient form on magnetic tape. A printed copy of the program in symbolic form together with the corresponding actual machine language is also produced. An example of the printout is shown in Figure 6.1-2. This is a section of the computer acceptance test program. The left-hand column indicates the absolute address of the storage location containing the data or instruction. The second, third, and fourth columns in the left-hand set form composite parts of the data or instruction, and the fifth column is the completed word, in octal format, and is the data actually stored inside the Micro D computer. The right-hand column is the symbolic language (source language).

The outputted magnetic tape is converted to paper tape to be read into the Micro D via the ground control equipment.

An assembler is also being written for use on the Micro D computer so that programs can be assembled via the teletypewriter. This will be used as a programming tool for assembling small engineering programs.

6.2 POWER SUPPLY

6.2.1 Introduction

All power required to operate the computer, computer interface, temperature control, sensor excitation, valve excitation, and monitors will be supplied by the power supply unit. The unit is functionally divided according to voltage, accuracy, and isolation requirements.

6.2.2 Supply Inputs

Electrical power for the HRE power supply will be derived from three sources:

A motor generator available for ground operations

B-52 power available for prelaunch operations

The two generator-turbine (APU) systems of X-15 for X-15 free-flight operations

```
                1000                            ORG 512
1000   34 0 0357 340357     MPRDO   DOT SECT8
1001   70 1 4164 720164             CLA MPRIN,1
1002   60 0 0240 600240             STA TCTR
1003   34 0 0306 340306             DOT SECT2
1004   70 1 1042 720042             CLA MPRCO,1
1005   60 0 0242 600242             STA RETAT
1006   70 1 1044 720044             CLA MPRCO+2,1
1007   60 1 1031 620031             STA MPRVI-1,1
1010   70 1 1045 720045             CLA MPRCO+3,1
1011   60 1 1032 620032             STA MPRVI,1
1012   70 1 1046 720046             CLA MPRCO+4,1
1013   60 1 1033 620033             STA MPRVI+1,1
1014   70 1 1043 720043             CLA MPRCO+1,1
1015   60 0 0241 600241             STA RETATX
1016   70 1 1032 720032     MPRMO   CLA MPRVI,1
1017   30 0 0253 300253             ADD THREE
1020   60 1 1032 620032             STA MPRVI,1
1021   60 0 0243 600243             STA SAVAR
1022   70 1 1031 720031             CLA MPRVI-1,1
1023   30 0 0253 300253             ADD THREE
1024   60 1 1031 620031             STA MPRVI-1,1
1025   70 1 1033 720033             CLA MPRVI+1,1
1026   30 0 0253 300253             ADD THREE
1027   60 1 1033 620033             STA MPRVI+1,1
1030   34 0 0357 340357             DOT SECT8
1031   70 1 4162 720162             CLA MPRIN-2,1
1032   14 1 4163 160163     MPRVI   MPR MPRIN-1,1
1033   30 1 4164 320164             ADD MPRIN,1
1034   60 0 0237 600237             STA SAVAC
1035   34 0 0251 340251             DOT ONE
1036   64 1 0330 660330             TRA TEST,1
1037   34 0 0306 340306     MPRSR   DOT SECT2
1040   64 0 1016 640016             TRA MPRMO
1041   64 1 0235 660235     MPREX   TRA RETEX,1
1042   00 0 1037 001037     MPRCO   PZE MPRSR
1043   00 0 1041 001041             PZE MPREX
1044   70 1 4162 720162             CLA MPRIN-2,1
1045   14 1 4163 160163             MPR MPRIN-1,1
1046   30 1 4164 320164             ADD MPRIN,1
```

Figure 6.1-2. (Sheet 1 of 2)

```
1047  34 0 0310 340310      ARSDO  DOT SECT5
1050  70 1 2554 720154             CLA ARSIN,1
1051  60 0 0240 600240             STA TCTR
1052  34 0 0306 340306             DOT SECT2
1053  70 1 1113 720113             CLA ARSCO,1
1054  60 0 0242 600242             STA RETAT
1055  70 1 1115 720115             CLA ARSCO+2,1
1056  60 1 1102 620102             STA ARSVI-1,1
1057  70 1 1117 720117             CLA ARSCO+4,1
1060  60 1 1104 620104             STA ARSVI+1,1
1061  70 1 1114 720114             CLA ARSCO+1,1
1062  60 0 0241 600241             STA RETATX
1063  70 1 1102 720102      ARSMO  CLA ARSVI-1,1
1064  30 0 0253 300253             ADD THREE
1065  60 1 1102 620102             STA ARSVI-1,1
1066  30 0 0251 300251             ADD ONE
1067  60 1 1075 620075             STA ARSVI-6,1
1070  60 0 0243 600243             STA SAVAR
1071  70 1 1104 720104             CLA ARSVI+1,1
1072  30 0 0253 300253             ADD THREE
1073  60 1 1104 620104             STA ARSVI+1,1
1074  34 0 0310 340310             DOT SECT5
1075  70 1 0000 720000             CLA **,1
1076  34 0 0306 340306             DOT SECT2
1077  30 1 1116 320116             ADD ARSCO+3,1
1100  60 1 1103 620103             STA ARSVI,1
1101  34 0 0310 340310             DOT SECT5
1102  70 1 2552 720152             CLA ARSIN-2,1
1103  40 0 0000 400000      ARSVI  ARS **
1104  30 1 2554 320154             ADD ARSIN,1
1105  60 0 0237 600237             STA SAVAC
1106  34 0 0251 340251             DOT ONE
1107  64 1 0330 660330             TRA TEST,1
1110  34 0 0306 340306      ARSSR  DOT SECT2
1111  64 0 1063 640063             TRA ARSMO
1112  64 1 0235 660235      ARSEX  TRA RETEX,1
1113  00 0 1110 001110      ARSCO  PZE ARSSR
1114  00 0 1112 001112             PZE ARSEX
1115  70 1 2552 720152             CLA ARSIN-2,1
1116  40 0 0000 400000             ARS **
1117  30 1 2554 320154             ADD ARSIN,1
```

Figure 6.1-2. (Sheet 2 of 2)

In all cases, the ac electrical system is a 400-cps, three-phase, four-wire, Y 115/200-v grounded neutral system, and the dc electrical system is a 28-vdc system.

The ground power units are in accordance with specification MIL-M-9397 and MIL-STD-704A. In cases of difference in specification, the design will treat the worst case condition. Where information is lacking in MIL-M-9797, MIL-STD-704A is assumed acceptable.

Due to lack of information about electrical power from B-52, MIL-STD-704A will be used. In cases where North American Aviation Inc. Report No. TFD59-233 states more extreme conditions than MIL-STD-704A, then it will be used.

Under X-15 free-flight conditions, the electrical power will be in accordance with MIL-STD-704A, NAS-4018, and MIL-E-7894. In any cases of inconsistencies, the most extreme limits will be the guide.

A comparison of MIL-STD-704A to any of the other specification mentioned will show that MIL-STD-704A is usually superior to any of the others with respect to extreme limits and completeness, and it will be the main guide followed throughout the supply design.

6.2.3 Supply Outputs

All power supplies required for the HRE control system electronics are dc voltage supplies. The total power requirement is shown in Table 6.2-1, the result of an overall system power estimate. As the table shows, the power supply will be divided in sections according to voltage, accuracy, and isolation requirements. Further supply grouping will be according to grounding sequence and power requirements.

The only power supply output requirements not mentioned in Table 6.2-1 are the power shutdown and turn-on sequence requirements which include transient behavior detection. This will be discussed more thoroughly in Para. 6.2.4.4.

6.2.4 Power Supply Circuitry

The initial block diagram (Figure 6.2-1) expresses the power distribution of Table 6.2-1. Due to grounding requirements, regulation, power specification, and monitoring, the entire supply will be grouped in four separate sections:

(a) Supplies using 28-vdc aircraft power.

(b) Supplies using 115-vac single-phase (1ϕ) aircraft power.

(c) Supplies using 115 vac three-phase (3ϕ) aircraft power.

(d) Total supply monitoring level detection, and turn-on/shutdown sequencing.

SUPPLY OUTPUT NUMBER	OUTPUT VOLTAGES	ACCURACY REQUIRE-MENT	MAXIMUM LOAD CURRENT	MINIMUM LOAD IMPEDANCE	EXPECTED LOAD REQUIRE-MENT CHANGES	POWER DELIVERED TO CONTROL SYSTEMS	INPUT POWER USED	GROUNDS OR REFER-ENCES	ISOLA-TION REQUIRE-MENTS
1	+28 VDC	±30%	1.000A	28Ω	±50%	28W	28 VDC	AIRCRAFT GROUND	———
2	+25 VDC	±2%	0.475A	52Ω	±20%	12W	28 VDC	SIGNAL GROUND	———
3	+15 VDC	±1%	2.815A	5.35Ω	±20%	43W	28 VDC	SIGNAL GROUND	———
4	-15 VDC	±1%	1.105A	13.6Ω	±20%	16W	28 VDC	SIGNAL GROUND	———
5	+10 VDC	±0.2%	0.120A	83Ω	±20%	1.2W	115 VAC-1φ	REF. NO. 1	COMPLETE ISOLATION
6	+10 VDC	±0.2%	0.120A	83Ω	±20%	1.2W	115 VAC-1φ	REF. NO. 2	COMPLETE ISOLATION
7	+5 VDC	±0.2%	0.200A	25Ω	±20%	1W	115 VAC-1φ	REF NO. 3	COMPLETE ISOLATION
8	+5 VDC	±5%	7.800A	0.64Ω	±20%	40W	115 VAC-3φ	SIGNAL GROUND	———

TABLE 6.2-1. SYSTEM POWER REQUIREMENTS

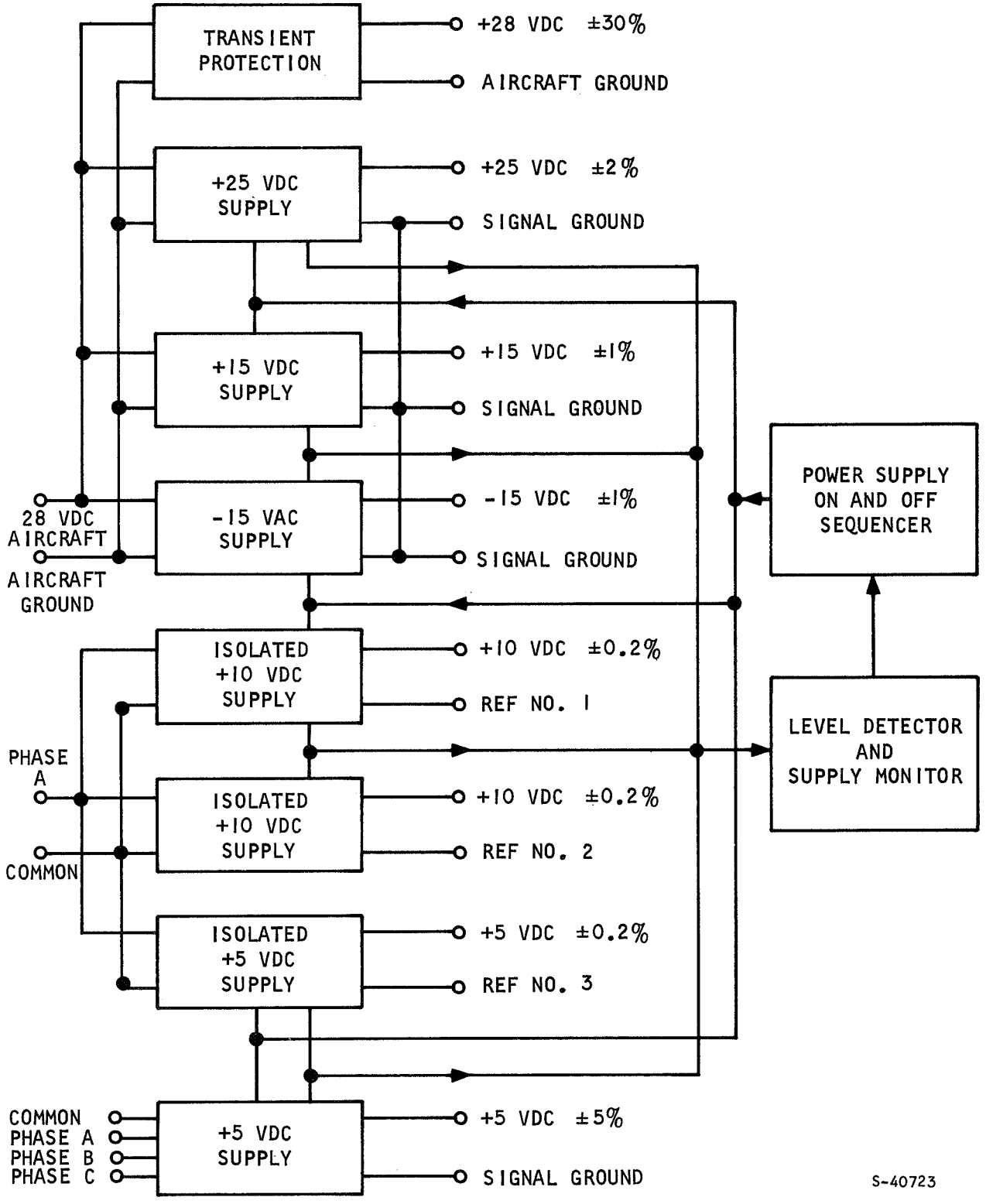


Figure 6.2-1. Initial Power Distribution and Monitoring Block Diagram

A final block diagram of part 6.2.4.1, 6.2.4.2, and 6.2.4.3 is represented in Figure 6.2-2. The following discussion outlines reasons for the power assignments shown in Figure 6.2-2.

Good regulation of supplies with high load currents depends on either very good filtering or regulated voltages which are at least a couple of volts lower than minimum source values. This implies a choice between producing good filters or operating with low power efficiencies.

By choosing to produce a well filtered system, we have the problem that frequencies as low as 400 cps for -115 vac single phase need enormous capacitors for energy storage.

A three-phase full-wave rectified system gives a dc output with less than 5 percent ripple without any filter. The ripple frequency is 6 x 400 cps and a filter of moderate size will reduce the ripple magnitude appreciably. This method appears to be best suited for the 5-vac, ±5-percent, 7.8-amp supply.

The +25 vdc, +15 vdc, and -15 vdc all need much better regulation than 5 percent. Since all of these carry heavy currents, the preferred method in these cases is to use high frequency dc to dc, frequency modulated, chopper supplies. The frequency modulation method was selected because of the long time transients specified for the 28-vdc aircraft power. The chopping frequency to be used will be between 10 kcps and 50 kcps. This will decrease the filter size to about 1/25 of that needed for the 400-cps, 115-vac, single-phase aircraft power.

The power consumption of the low current, highly regulated supplies will be much lower than any of the other supplies. So by designing these with the output voltages several volts lower than the source signal values the power losses due to regulation will still be negligible, and filtering will not be as critical as for the other supplies. Total isolation is a requirement for the highly regulated supplies. The most suitable solution for these supplies is to use 115-vac, 400-cps single-phase power since the total power requirement is quite small.

The ARMA Micro-D computer used in the fuel control system has very tight specifications for short-circuit and overvoltage protection. For operation outside the tolerable limit, the computer must have its power inputs sequenced off in a certain way. Because of the time limits for overvoltage and short circuits, level detection must be used and action must be taken before the operating limits are reached. This is done using sufficient storage capacity and proper time delays in the supply filters and regulators.

The power layout gives certain level detection advantages. Examination of the voltage supplies are used to supply the computer its +25 v, +15 v, -15 v, and 5 v (±5 percent) shows that the +25 v, +15 v, and -15 v will all have a common level detector on the 28-vdc aircraft power. This provides the required time delay to turn the supplies off before the outputs pass the proper limits, in cases of adverse conditions. The 5-v (±5 percent) supply

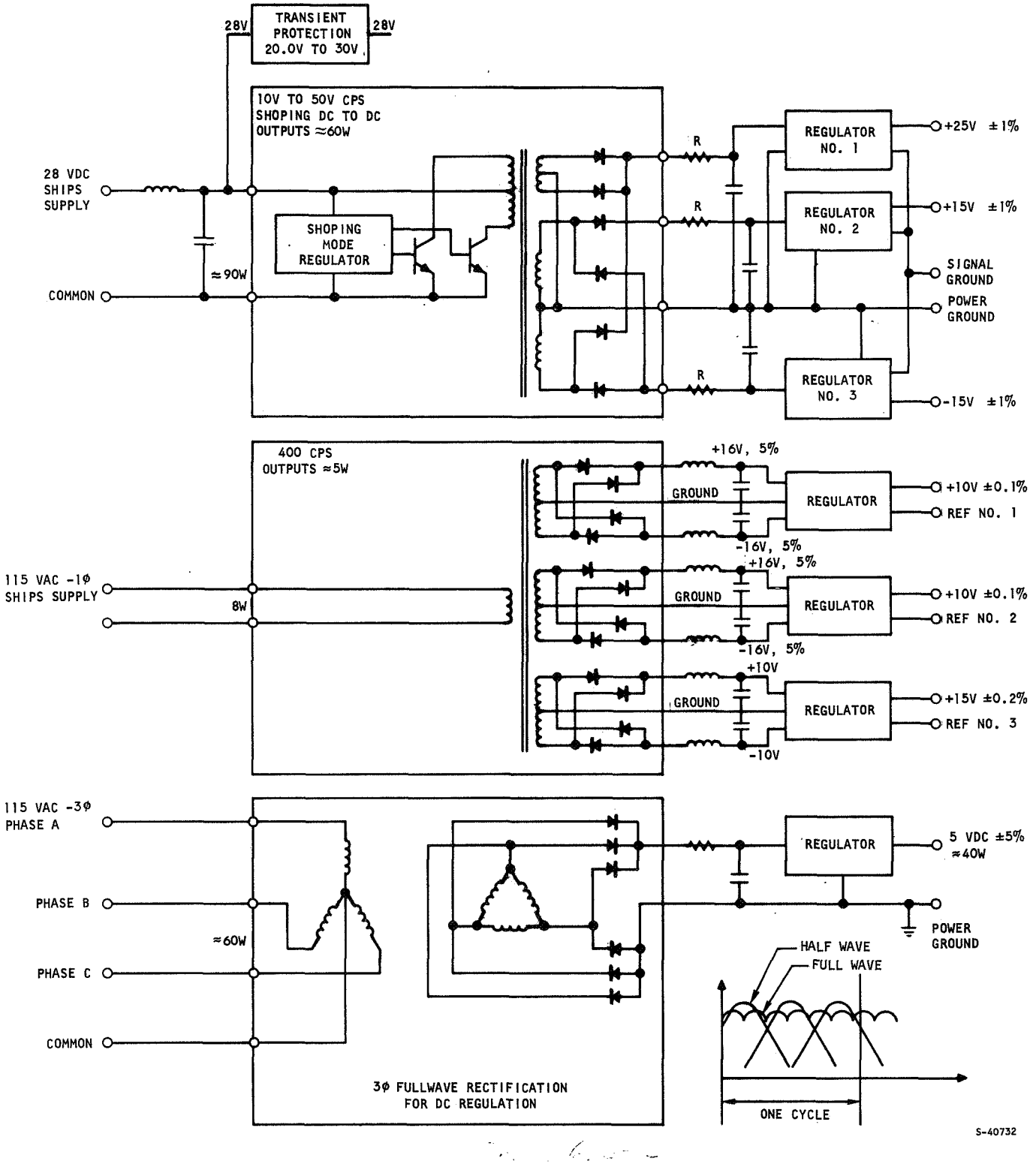


Figure 6.2-2. Power Distribution Block Diagram

will have the level detection prior to the filter (on the fullwave rectifier output) which is a dc voltage with less than 5-percent ripple, and the filter will provide the time delay needed for the supply to turn off. The highly regulated supplies have no given level detection specifications. However, failure monitoring for these outputs and other supply outputs will be needed due to HRE fail-safe operating requirements.

6.2.4.1 Supplies Using 28-vdc Aircraft Power

The 28-vdc aircraft system specification for steady state is over the range of 17 vdc to 30 vdc. The long time transient condition lasts for as long as 5 sec and a limit of 80 v for 0.5 ms. Voltage spike limits are 600 v for a duration not to exceed 50 μsec.

To accommodate the 80 v transient without using an enormous filter, the supply is designed to function with inputs between +17 vdc and +80 vdc. This will be accomplished by a frequency-modulated preregulator which will provide a preferred secondary voltage within ±25 percent. An input-protected final regulator will regulate the output to ±1 percent. This method is used for all three supplies: +25 vdc ±2 percent, +15 vdc ±1 percent, and -15 vdc ±1 percent. They will all be controlled by the same preregulator and each with their own final regulators. Figure 6.2-3 shows the block diagram of the +25-v, +15-v, and -15-v supply section.

The block diagram of the preregulator is shown in Figure 6.2-4. Operating waveforms of the preregulator are shown in Figure 6.2-5.

T_2A is the on time of Q9, and T_2B is the on time of Q10, while both are off through time T_1. Total time $T_1 + T_2 = \text{Const} = \frac{1}{f}$ where f is the frequency of the oscillator (multivibrator).

Neglecting transformer errors and filtering errors we have

$$E_{out} = C_1 \times \frac{T_2 \times E_{in}}{(T_1 + T_2)} = C_2 \times T_2 \times E_{in}$$

where: C_1 and C_2 are both constants with $C_2 = \frac{C_1}{[T_1 + T_2]}$

C_1 is a function of transformer ratio and the preadjusted duty cycle of the switching.

The only element that controls the duty cycle and thereby the output voltage is the one shot. By using a changeable current I_{C5}, which is a linear function of the input voltage, to charge up the time controlling capacitor of the one shot, we have linear regulation on the duty cycle of the switching transistors Q9 and Q10.

The preregulator circuitry is shown in Figure 6.2-6. The changeable current I_{C5} is produced by the circuitry CR5, R11, R12, R13, and Q6. The time controlling capacitor of the one shot is C5. Some initial breadboard tests of the preregulator are shown in Figures 6.2-7, 6.2-8 and 6.2-9. These pictures show the actual waveforms taken under test to verify the operations shown in Figure 6.2-5.

Figure 6.2-7 shows tests taken at -55°C.

Figure 6.2-8 shows tests taken at +25°C.

Figure 6.2-9 shows tests taken at +125°C.

Figure 6.2-10 shows the preregulator breadboard.

The final regulation of +25 v, +15 v, and -15 v uses hybrid circuit voltage regulators. The regulators are Amelco Semiconductor Products identified as 2802Bg for positive regulators and 2803 for negative regulators. Both types of regulators are packaged in low-profile TO8 headers. They can provide 0.1 percent load and line regulation and 0.5 percent stability from -65°C to +125°C. They are capable of controlling load currents as high as 10 amp with an external transistor. The final regulators are shown in the schematic Figure 6.2-11. The regulators 2802BG (A3 or A4) and 2803BG (A5) need overvoltage protection for voltages exceeding 55 v. Input circuits (Q11, R22 and CR12) provide this protection by limiting the input voltage to the zener voltage V_{CR12} = 50 v.

The regulators have differential amplifiers in the feedback path. For accurate operation, a differential amplifier needs a good reference. This is accomplished by components CR15 and CR16. The differential amplifiers are connected as shown in Figure 6.2-12.

Resistor R28 is trimmed to set the output voltage to any value from 4.5 v to 40 v. The only limitation to this setting is that the input voltage must be at least 2.5 v higher than the output value. Figure 6.2-13 shows the initial breadboard of the "final regulators."

Figure 6.2-14 shows the initial breadboard test set up for the complete +25 v, +15 v, and -15 v, supplies.

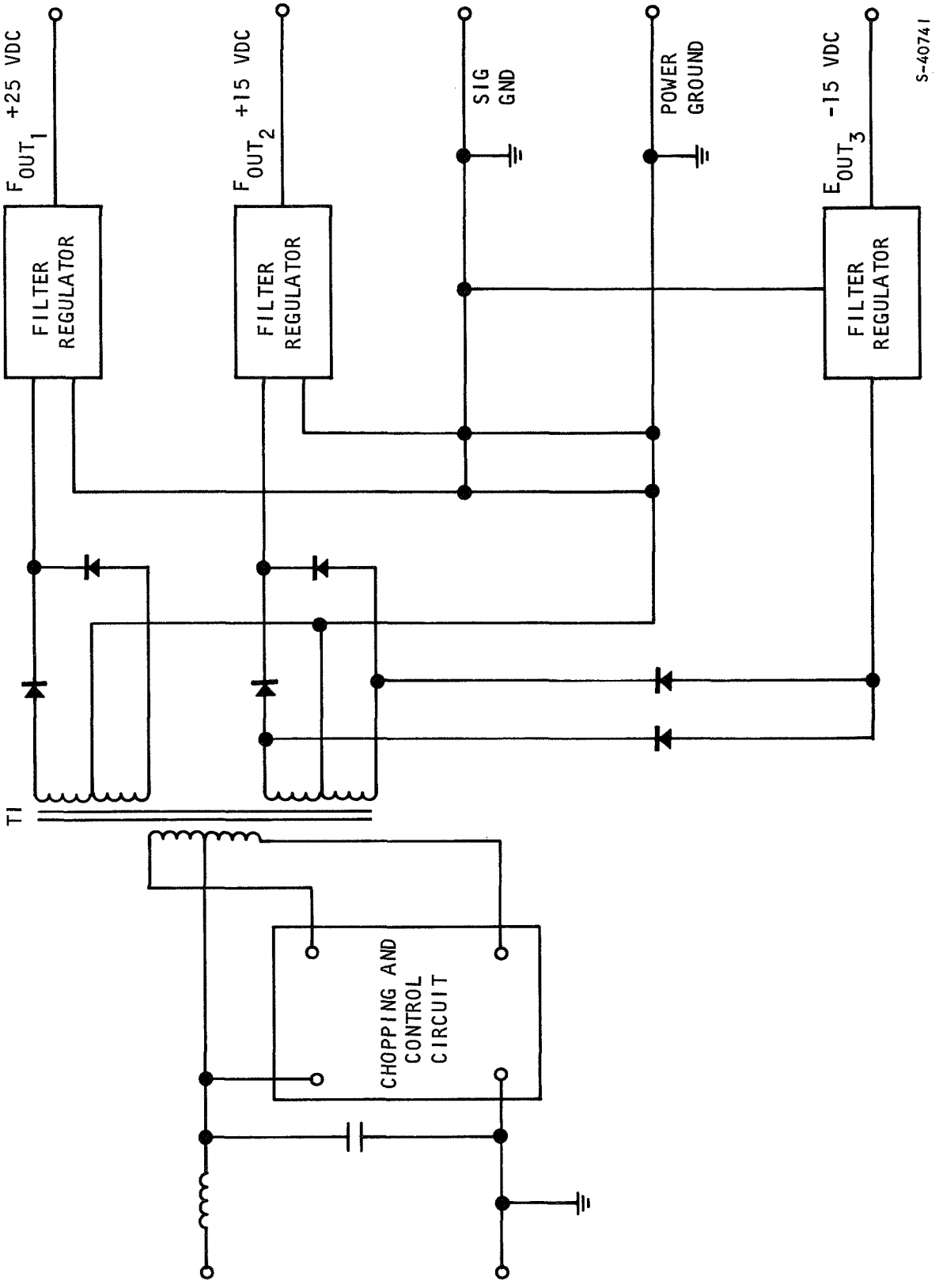


Figure 6.2-3. +25 V, +15 V, and -15 V to al Block Diagram

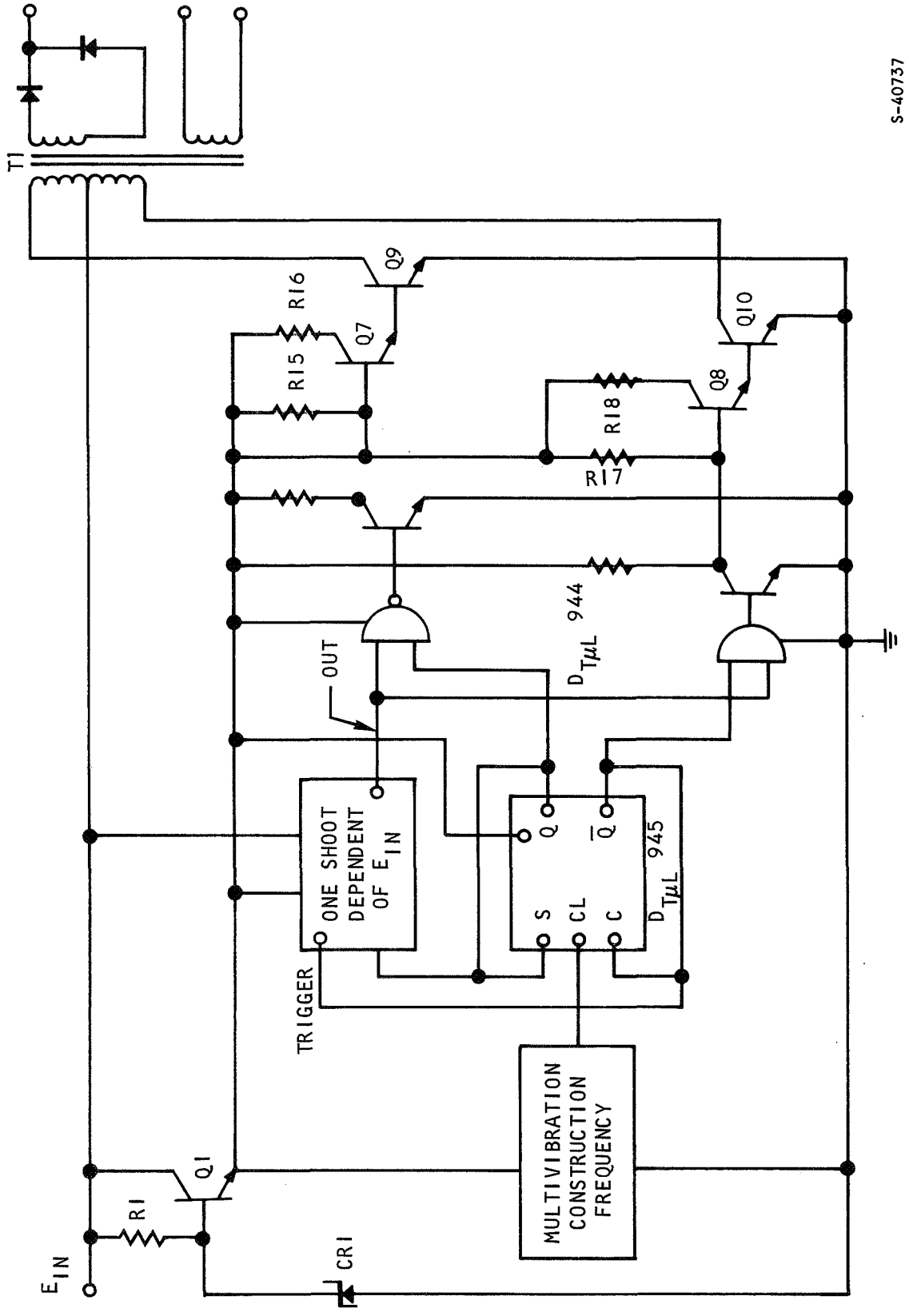


Figure 6.2-4. +25 V, +15 V, and -15 V Preregulator

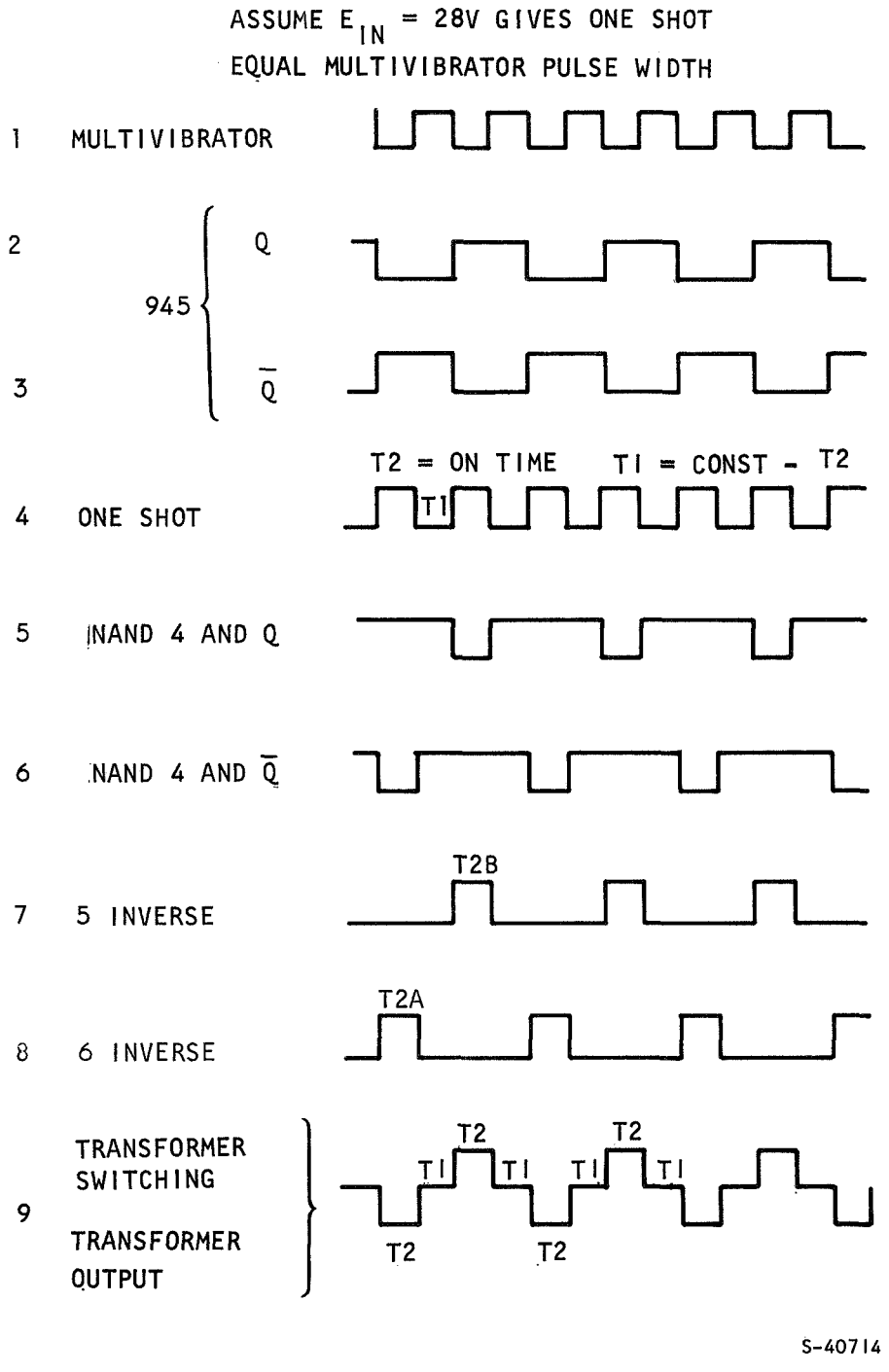


Figure 6.2-5. Preregulator System Operation

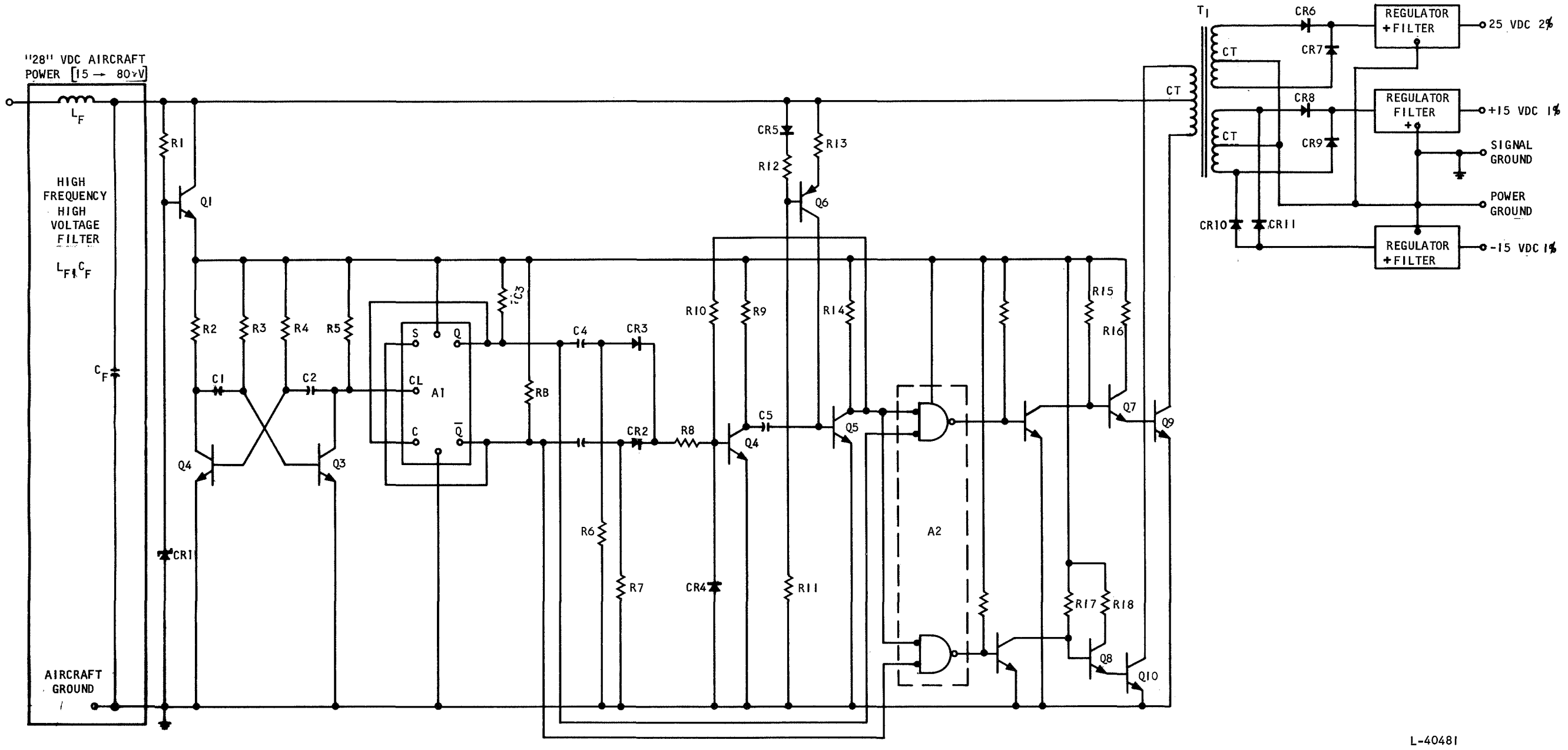


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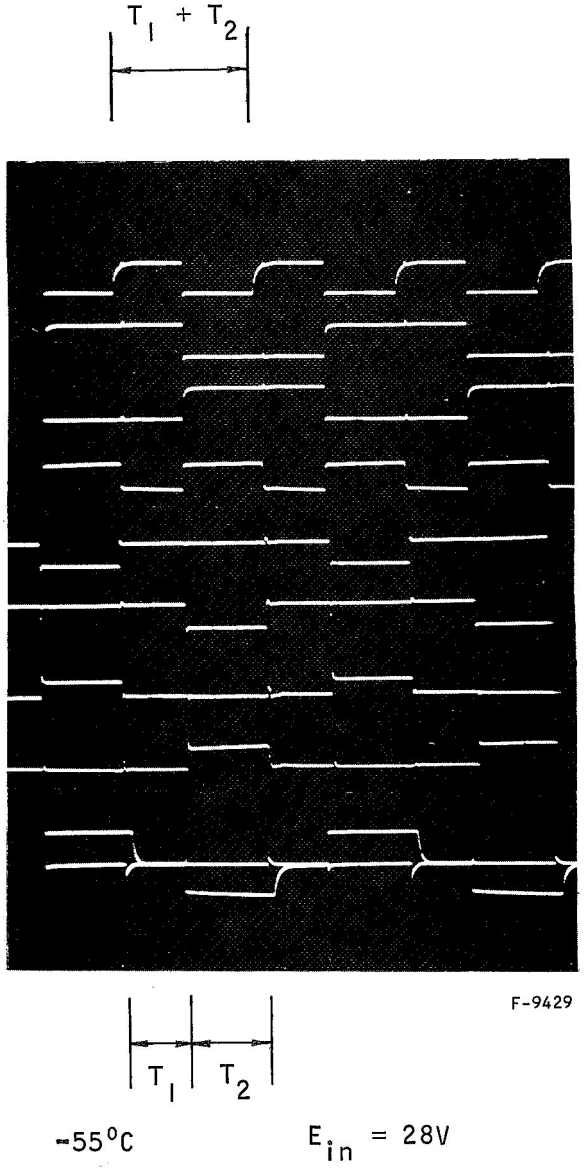
Figure 6.2-6. Preregulator Circuitry

PARTS LIST FOR FIGURE 6.2-6

R1 = 1 K Ω ± 5 percent, 2 w
R2 = 600 Ω ± 5 percent, 1-1/4 w
R3 = 12 K Ω ± 1 percent, 1/4 w
R4 = 12 K Ω ± 1 percent, 1/4 w
R5 = 600 Ω ± 5 percent, 1/4 w
R6 = 1 K Ω ± 5 percent, 1/4 w
R7 = 1 K Ω ± 5 percent, 1/4 w
R8 = 2 K Ω ± 5 percent, 1/4 w
R9 = 200 Ω ± 5 percent, 1/4 w
R10 = 10 K Ω ± 5 percent, 1/4 w
R11 = 500 K Ω ± 1 percent, 1/4 w
R12 = 125 K Ω ± 1 percent, 1/4 w
R13 = 10 K Ω ± 1 percent, 1/4 w
R14 = 1 K Ω ± 1 percent, 1/4 w
R15 = 100 Ω ± 5 percent, 1/4 w
R16 = 5 Ω ± 5 percent, 5 w
R17 = 100 Ω ± 5 percent, 1/4 w
R18 = 5 Ω ± 5 percent, 5 w
RA = 510 Ω ± 5 percent, 1/4 w
RB = 510 Ω ± 5 percent, 1/4 w
C1 = 1200 pf ± 1 percent, 20 v (25 ppm cc)
C2 = 1200 pf ± 1 percent, 20 v
C3 = 2000 pf ± 10 percent 20 v
C4 = 2000 pf ± 10 percent, 20 v
C5 = 1000 pf ± 1 percent, 50 v
CF =
LF =
CR1 = IN387FA (or ± 2 percent is better)
CR2 = IN457 (70 w diode)
CR3 = IN457
CR4 = IN457
CR5 = IN457
CR6 = UT4020 (200 v diode) Unitrode
CR7 = UT4020
CR8 = UT4010
CR9 = UT4010
CR10 = UT4010
CR11 = UT4010
Q1 = 2N3236 (or 2N3055)
Q2 = 2N910
Q3 = 2N910
Q4 = 2N222
Q5 = 2N222
Q6 = 2N3064 (65)
Q7 = 2N3036
Q8 = 2N3036
Q9 = 2N3236 (or 2N3055)
Q10 = 2N3236 (or 2N3055)
QA = 2N222
QB = 2N222
A1 = DTμL 945
A2 = DTμL 944



(1) MULTIVIBRATOR

(2) $D_{T\mu L}$ 945 Q

(3) $D_{T\mu L}$ 945 $\overline{Q}$

(4) ONE SHOT

(5) NAND 4 AND Q

(6) NAND 4 AND $\overline{Q}$

(7) 5 INVERSE

(8) 6 INVERSE

(9) TRANSFORMER SWITCHING Q9-Q10

Figure 6.2-7. Preregulator System Operation Tested at -55°C

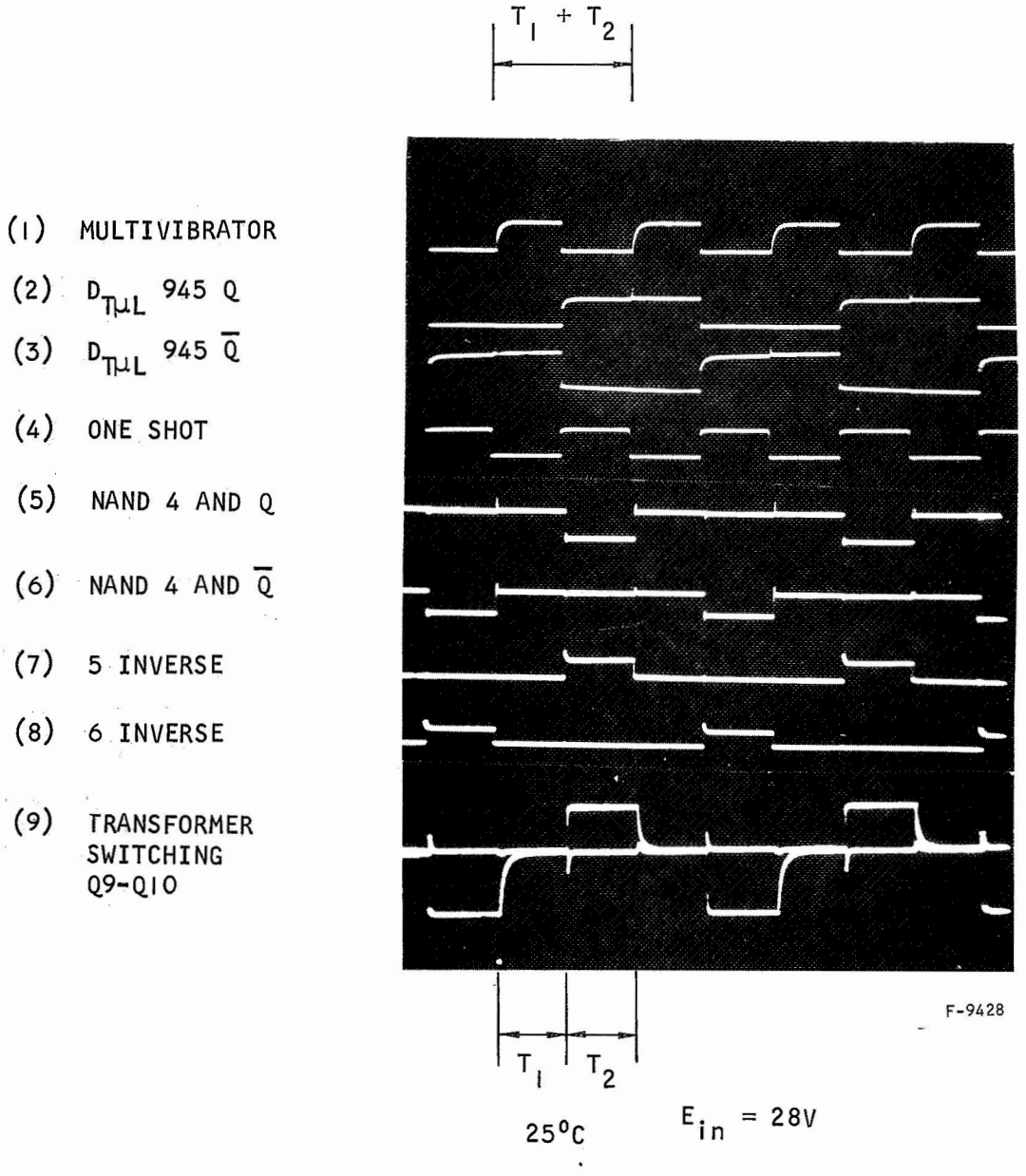


Figure 6.2-8. Preregulator System Operation Tested at +25°C (Room Temperature)

(1) MULTIVIBRATOR

(2) $D_{T\mu L}$ 945 Q

(3) $D_{T\mu L}$ 945 $\overline{Q}$

(4) ONE SHOT

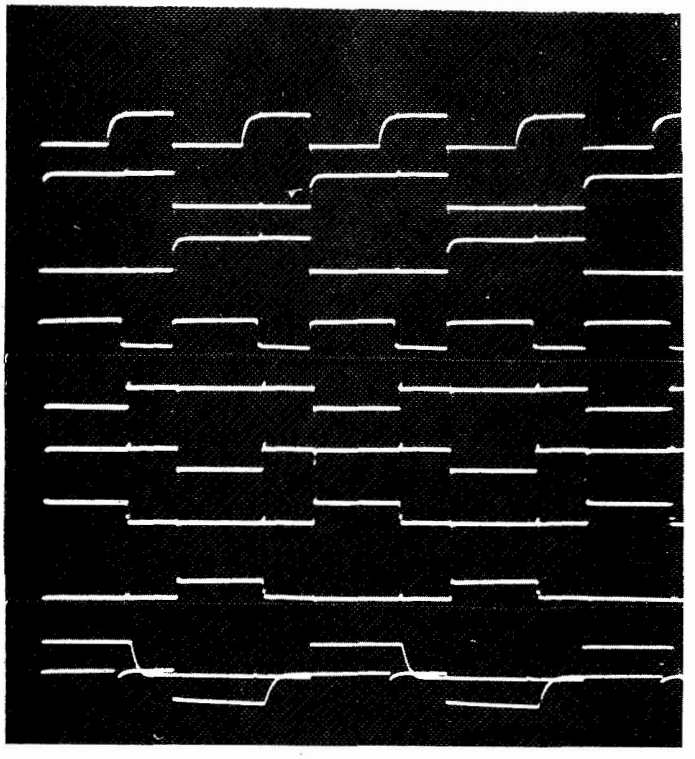
(5) NAND 4 AND Q

(6) NAND 4 AND $\overline{Q}$

(7) 5 INVERSE

(8) 6 INVERSE

(9) TRANSFORMER SWITCHING Q9-Q10



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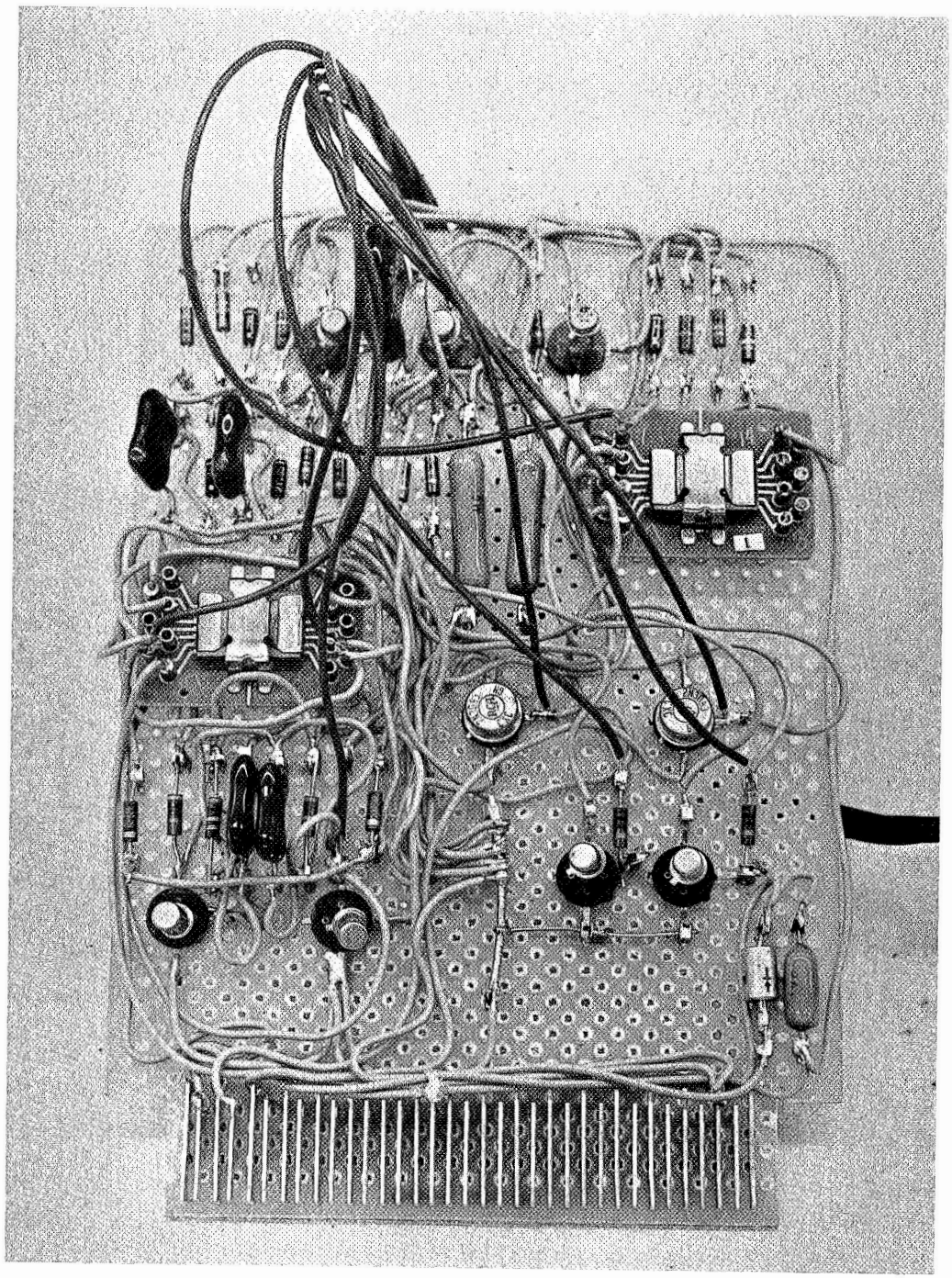
$125^{o}C$ E_{in} = 25V

Figure 6.2-9. Preregulator System Operation Tested at $+125^{o}C$



F-9381

Figure 6.2-10. Preregulator Breadboard

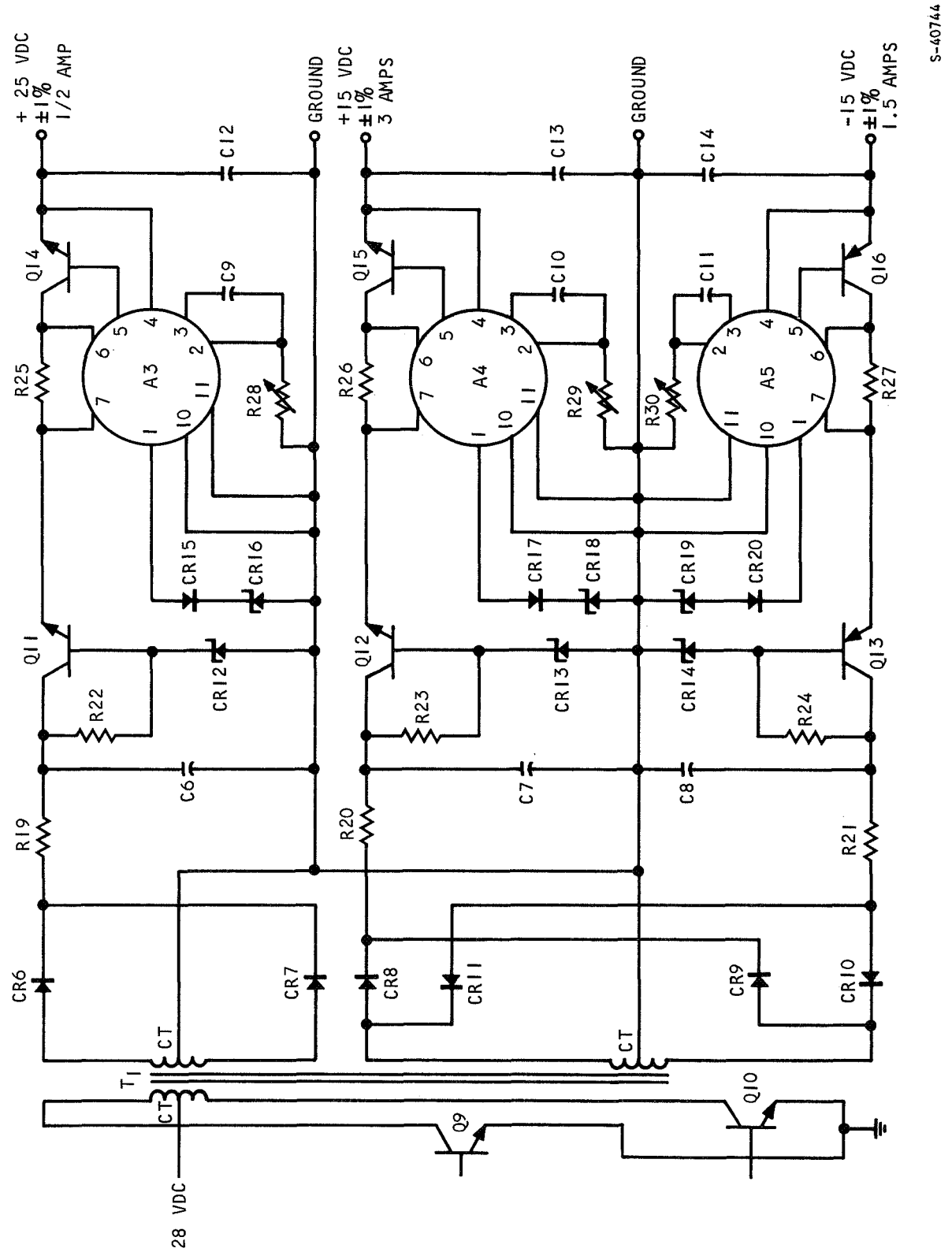


Figure 6.2-11. Final Regulators for +25 V, +15 V, and -15 V

PARTS LIST FOR FIGURE 6.2-11

R19 = 10 Ω ± 5 percent, 5 w (200 v)

R20 = 1 Ω ± 5 percent, 35 w (0 Ω?)

R21 = 25 Ω ± 5 percent, 20 w (0 Ω?)

R22 = 51 Ω ± 5 percent, 1/2 w

R23 = 10 Ω ± 5 percent, 3 w

R24 = 10 Ω ± 5 percent, 3 w

R25 = 1/2 Ω ± 5 percent, 1 w

R26 = 0.1 Ω ± 5 percent, 3 w

R27 = 0.2 Ω ± 5 percent, 2 w

R28 = 5 K Ω presition P_{QT} (actual value 3.6 K Ω ± 0.1%)

R29 = 50 K Ω P_{QT} (actual = 30 K Ω)

R30 = 50 K Ω P_{QT} (actual = 30 K Ω)

C6 = 10 μf ± 100 percent, 150 v (with f = 50,000) (50 μf for f = 10,000)

C7 = 60 μf ± 100 percent, 150 v (with f = 50,000)

C8 = 30 μf ± 100 percent, 150 v (with f = 50,000)

C9 = 47 μf ± 10 percent, 50 v

C10 = 47 μf ± 10 percent, 50 v

C11 = 47 μf ± 10 percent, 50 v

C12 = 10 μf

C13 = 10 μf

C14 = 10 μf

CR6 = UT4020 Unitrode power diode

CR7 = UT4020 Unitrode power diode

CR8 = UT4010 Unitrode power diode

CR9 = UT4010 Unitrode power diode

CR10= UT4010 Unitrode power diode

CR11= UT4010 Unitrode power diode

CR12= UZ5850 Unitrode zener diode

CR13= UZ5850 Unitrode zener diode

CR14= UZ5850 Unitrode zener diode

CR15= IN457

CR16= IN3514

CR17= IN457

CR18= IN3514

CR19= IN3514

CR20= IN457

Q11 = 2N3236

Q12 = 2N3236

Q13 = 2N3789

Q14 = 2N3236

Q15 = 2N3236

Q16 = 2N3789 (substitute 2N3741)

A3 = 2802Bg Amelco hybrid voltage regulator

A4 = 2802Bg Amelco hybrid voltage regulator

A5 = 2803Bg Amelco hybrid voltage regulator

T_1 = ADC-S1846 (by ADC Electronics)

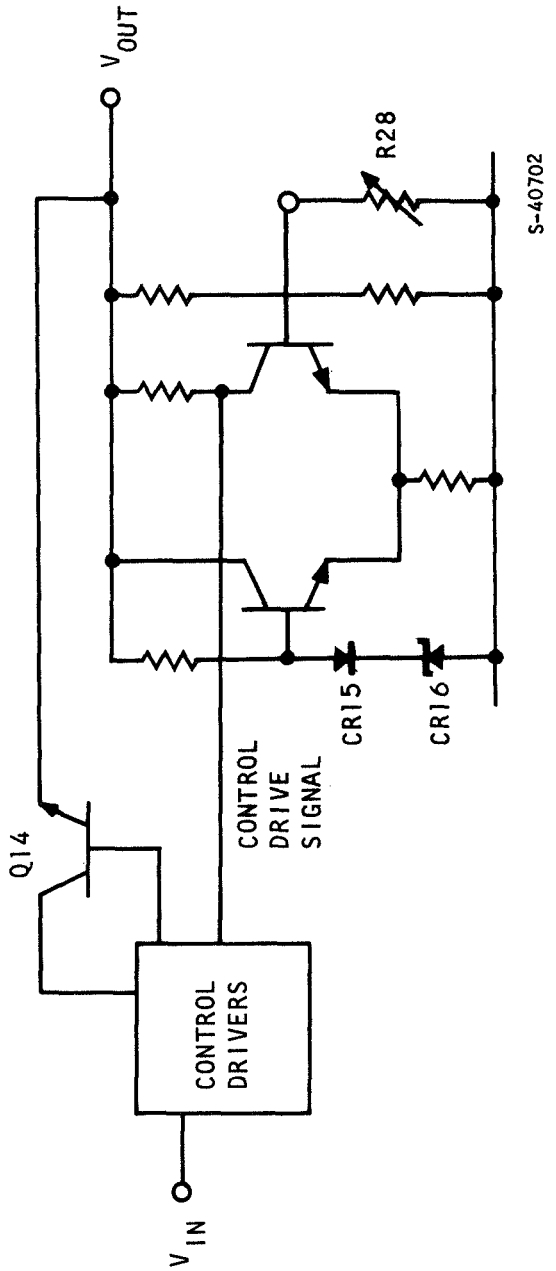


Figure 6.2-12. Differential Amplifier Connections

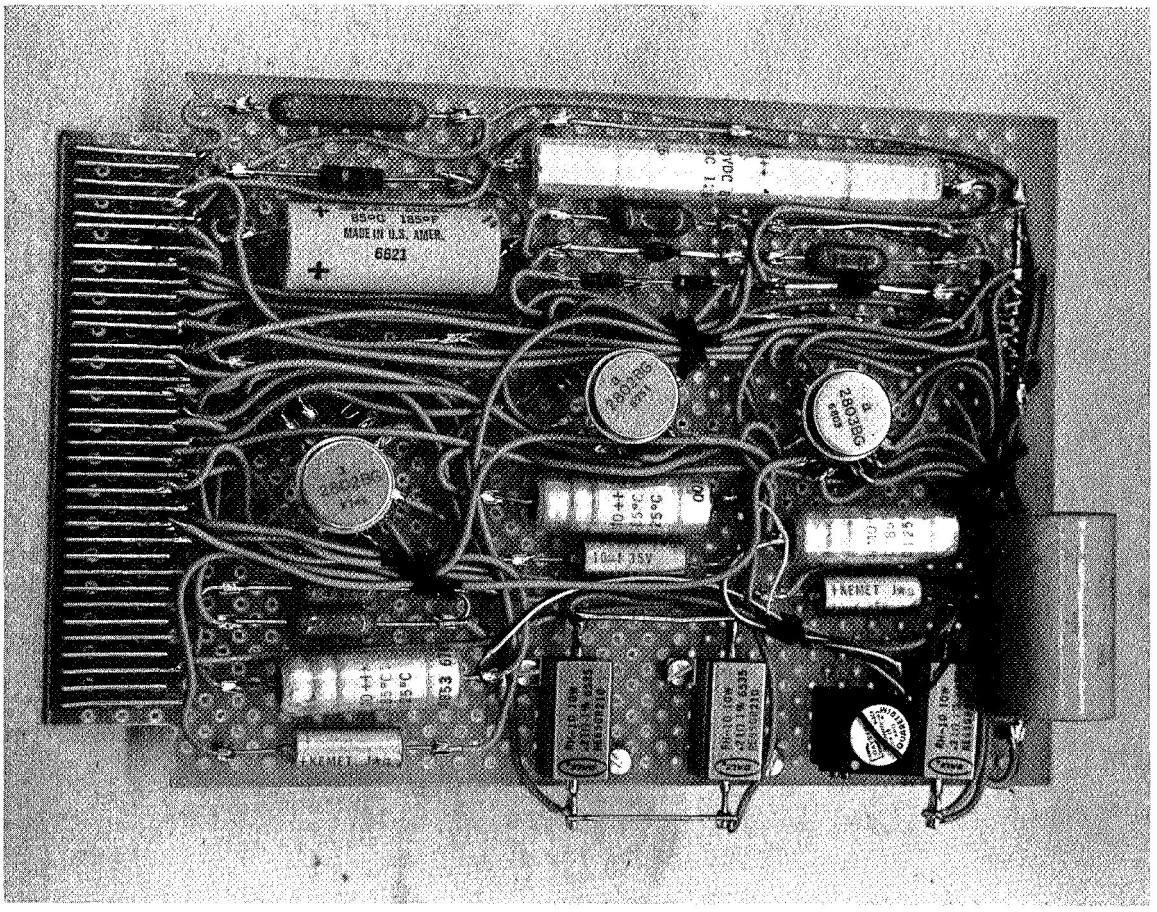
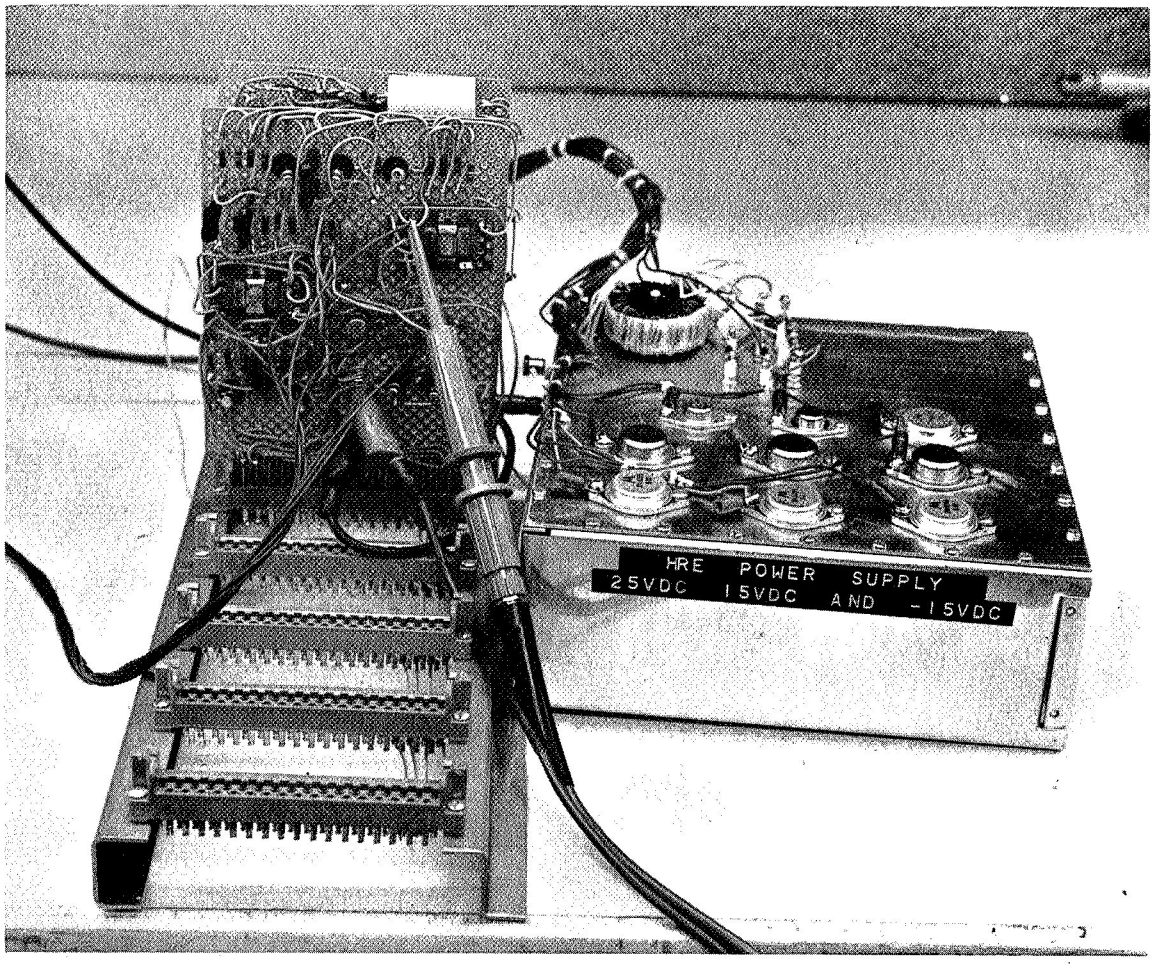


Figure 6.2-13. Initial Breadboard of Final Regulators



F-9379

Figure 6.2-14. Initial Breadboard Test Setup for Complete +25 v, +15, and -15 v Supplies

6.3 COMPUTER INTERFACE ANALOG SECTION

6.3.1 Computer Interface Unit (CIU)-Digital Section

During this reporting period the digital portion of the CIU has been substantially completed and integrated into a cabinet containing both stimuli and display facilities. The equipment has been tested and found to function correctly, though the hardware must still be subjected to extensive environmental and dynamic performance checks.

It should be noted that since the remainder of the interface system is undergoing either definition, design, or construction, the digital portion of the interface is a first-order design. The design cannot be completed and refined until the system as a whole has been completed, integrated with the computer, and checked out dynamically with simulated inputs and outputs.

Digital circuitry which has been checked out functionally will have been interfaced with the computer by the end of April 1968. It will then be possible to perform limited programming development with the I/O system.

The following subsections describe in detail the operation of the digital CIU, illustrated in Figure 6.3-1.

Figures 6.3-2, 6.3-4, 6.3-7, and 6.3-8 show circuits of the digital portion of the CIU, and Figures 6.5-1, 6.5-2, 6.5-3, and 6.5-4 illustrate the breadboard hardware and the integrated rack-assembly.

6.3.1.1 CIU Operation

The third TDR explained the principle of the operation of CIU.

The configuration of the CIU has changed with regard to the multiplexing technique as a result of further tradeoff considerations. Solid-state switch multiplexing rather than comparator-multiplexing is proposed, this technique is illustrated in Figure 33 of the third TDR.

To simplify the description of the operation of the digital equipment, the CIU is divided into areas corresponding to the actual circuit boards, namely the interface control logic, ADC logic and I/O transfer register, and the multiplexer decoder.

To assist in the explanation of the operation of the interface control logic, and for convenient reference purposes, the input/output instructions are listed in the following paragraphs.

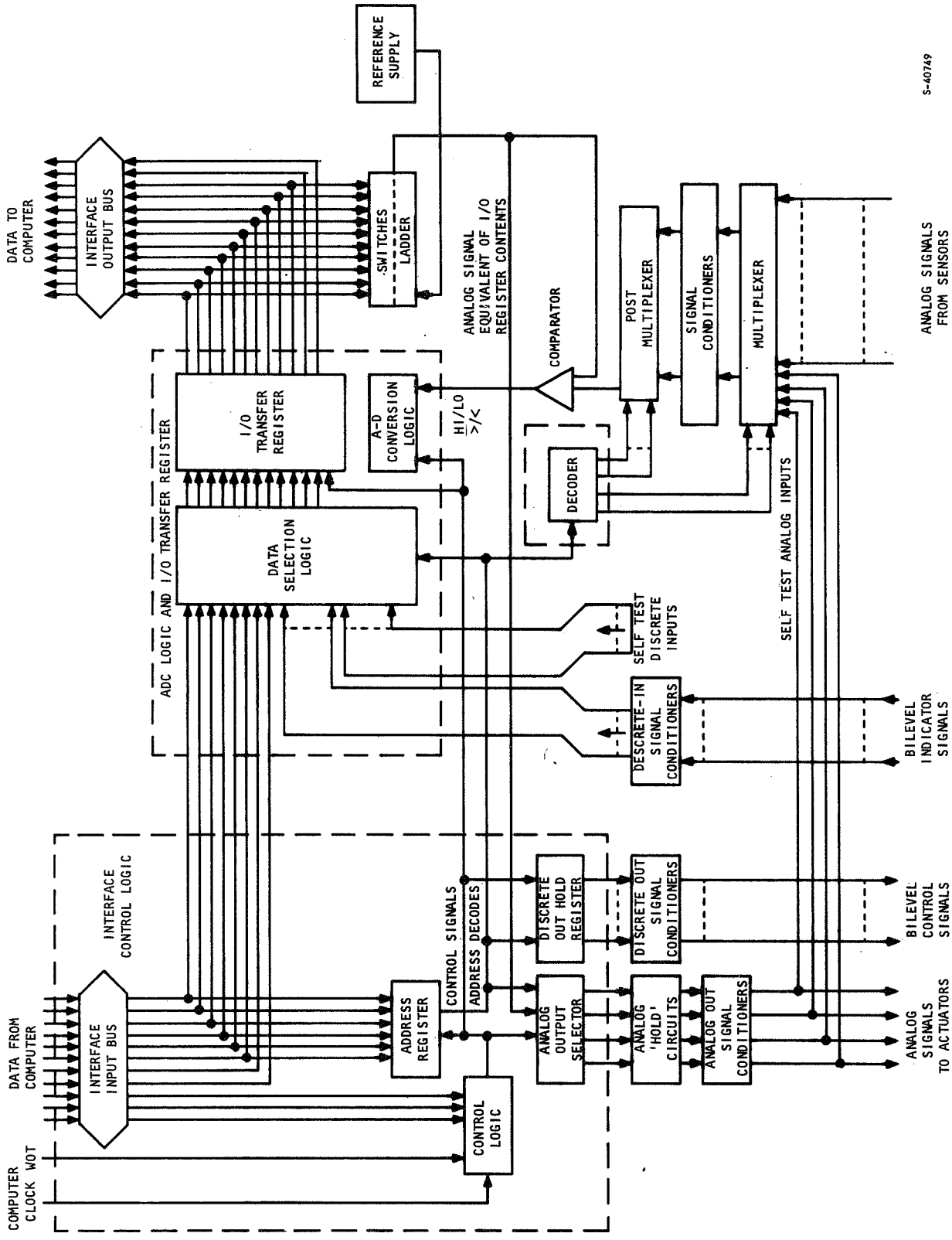


Figure 6.3-1. Fuel Control System, Computer Interface Unit

6.3.1.2 Input/Output Instructions

There are three basic I/O instructions available in the ARMA Micro-D computer. These are the WOT (Word Out), DOT (Data Out), and DIN (Data In). The interface unit (Figure 6.3-1) recognizes only the WOT instruction which provides an 18-bit computer data word to the interface unit. This 18 bit word is interpreted by the interface unit to provide the data input/output necessary for fuel control. At present, only 11 of the 18 bits are utilized. The general format is as follows:

18	17	16	15	14	13	12 11 10 9	8	7	6	5	4	3	2	1
NOT USED			X	X	X	NOT USED	X	X	X	X	X	X	X	X
			Opcode				Data/Address							

The three opcode function bits (bits 13, 14, 15) identify to the CIU the operation to be performed. Bits 16 through 18 are available for expansion of the function codes. The 8 data/address bits depend on the function code for their interpretation. The following functions are currently defined.

Function	Code	Operation
0	000	Analog data output
1	001	Analog data input
2	010	Discrete data input
3	011	Select analog out address
4	100	Not assigned
5	101	Set discrete out
6	110	Reset discrete out
7	111	Not assigned

6.3.1.2.1 Setup of Analog Input

Bit position	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Content	NOT USED			0	0	1	NOT USED						X	X	X	X	X	X
				Opcode									Address					

Address Assignments: Individual sensor address assignements can be arranged by the programmer, but have been tentatively arranged as shown below:

Sensors	Addresses (Octal)	
Pressure	00-06, 10-16, 20-26, 30-36, inclusive	48
Temperature	40-42, 50-52, inclusive	
Miscellaneous	60-62, 70-72, inclusive	
Unused	07, 17, 27, 37, and 43-47, 53-57, 63-67, 73-77, inclusive	24

Operation: The addressed sensor output is converted to a positive binary number. The word length of the converted value is 10 bits. The number is available to the computer in the least significant bit positions of the 18 bit computer word. Unused bits will be held "false" (0). Update of analog outputs is terminated by this instruction.

Time: The converted value may be sampled via a DIN instruction 126 μsec* after execution of the WOT instruction. In the interval between execution of the WOT and DIN instructions, other WOT instructions may not be executed.

6.3.1.2.2 Setup of Discrete Input

Bit position	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Content	NOT USED			0	1	0	NOT USED									X	X	X
				Opcode												Address		

Address Assignments: Each address selects 12 discretes. Two addresses have been assigned, one for external and one for internal or self test, discretes.

Input	Address
External Discretes In	1 001
Self-Test Discretes In	2 010

The assignment of bit positions for individual discretes may be made by the programmer.

* 126 μsec equals seven computer word-times.

Operation: The addressed set of discretes is clocked into the I/O register. Update of analog output is terminated by this instruction.

Time: The discretes may be sampled via a DIN instruction immediately following the WOT instruction. If an interval is left between the WOT-DIN instructions, other WOT instructions may not be executed during this interval.

6.3.1.2.3 Setup of Analog Output Address

Bit position	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Content	NOT USED			0	1	1	NOT USED									X	X	X
				Opcode												Address		

Address Assignments: Current requirements specify four analog outputs Specific assignment of the analog addresses (0-7) to each of the four outputs may be made by the programmer.

Operation: The I/O register is cleared and the address placed in the address register. Update of analog outputs is terminated by this instruction.

Time: This instruction requires no programmed delay. It may be immediately followed by the analog data output.

6.3.1.2.4 Setup of Analog Output Data

Bit position	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Content	NOT USED			0	0	0	NOT USED				X	X	X	X	X	X	X	X
				Opcode							Data							

Address Assignments: Output address previously setup by analog output address select WOT instruction.

Operation: This instruction is preceded by an analog output address select WOT (bits 15, 14, 13 = 011) which determines the output to be updated. The 8-bit data value is clocked into the I/O register. The updating process will be enabled and continue enabled until another WOT instruction is executed.

Time: Worst-case slewing requirements for the output holding capacitors require a minimum dwell time of one millisecond. Hence another WOT instruction may not be executed for a period of at least 1 ms following execution of this instruction.

6.3.1.2.5 Set Discrete Output

Bit position	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Content	NOT USED			1	0	1	NOT USED				X	X	X	X	X	X	X	X
	Opcode										Address							

Address Assignments: Addresses may be assigned by the programmer. Addresses correspond to the eight discretes as shown in the table below.

	Address							
Discrete	8	7	6	5	4	3	2	1
0	1	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	1	0	0
4	0	0	0	0	1	0	0	0
5	0	0	0	1	0	0	0	0
6	0	0	1	0	0	0	0	0
7	0	1	0	0	0	0	0	0
All	1	1	1	1	1	1	1	1

The address for each discrete must be the same for both this instruction and for the Reset Discrete Out WOT instruction.

Operation: Execution of this instruction unconditionally sets the addressed discrete to its true (1) voltage level. Other discretes are unaffected. Update of analog outputs is terminated by this instruction.

Time: This instruction requires no programmed delay. It may be immediately followed by any other instruction.

6.3.1.2.6 Reset Discrete Output

Bit position	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Content	NOT USED			1	1	0	NOT USED				X	X	X	X	X	X	X	X
	Opcode										Address							

Address Assignment: The address for each discrete must be the same for both this instruction and for the Set Discrete Output WOT instruction.

Operation: Execution of this instruction unconditionally resets the addressed discrete to a "False" (0) voltage level. Other discretes are unaffected. Update of analog outputs is terminated by this instruction.

Time: This instruction requires no programmed delay. It may be immediately followed by any other instruction.

6.3.1.3 Computer Interface Control Logic

The interface control logic is illustrated in Figure 6.3-2. The circuit has been subdivided into seven functional areas, namely:

Clock-dividers

Computer instruction detector and transfer control sequencer

Operation code (Opcode) memory and decoder, transfer control

Signal generator

Computer-output address/data bus

Address-memory and decoder

Discrete output signal memory

ADC start-conversion delay circuit

The function of this portion of the system is to interpret the computer instructions (requiring the input or output of data) and to generate the necessary timing and control signals for the remainder of the system. Further, memory elements are provided to retain instructions during execution to "free" the computer after each instruction transfer is made (with the exception of analog outputs). Memory elements are also provided to retain the states of the discrete output signals. The operation of the seven functional areas are described below.

6.3.1.3.1 Clock Dividers

The clock dividers receive the computer 1.5 MHz clock-pulse-train, which is approximately 1:3 mark:space ratio. The signal is buffered by a gate to provide a standard load at the computer output interface. The three binary dividers are synchronously clocked to minimize skew in the resulting system clocks. The three dividers produce clocks at 750 KHz, 375 KHz, and 187.5 KHz. The first division-by-two assures that all clocks have a 1:1 mark:space ratio. The clocks are referred to as f_1, f_2, and f_3 respectively.

The timing of the CIU is shown in Figure 6.3-3. Due to the arbitrary relationship of the computer WOT signal relative the clocks in the CIU, a number of possible signal relationships are possible and these are shown in Figure 6.3-3 with dotted lines.

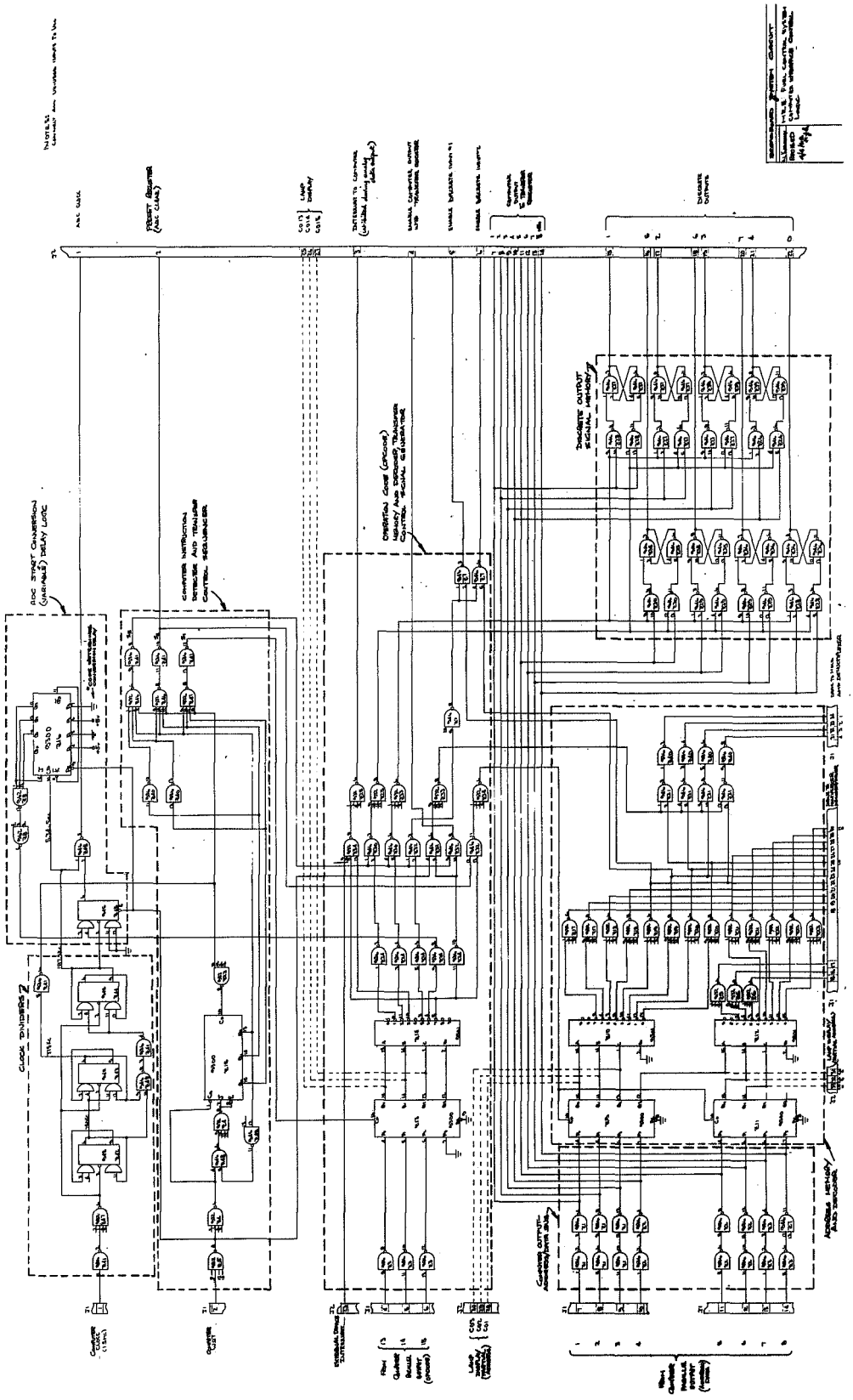


Figure 6.3-2. Computer Interface Control Logic

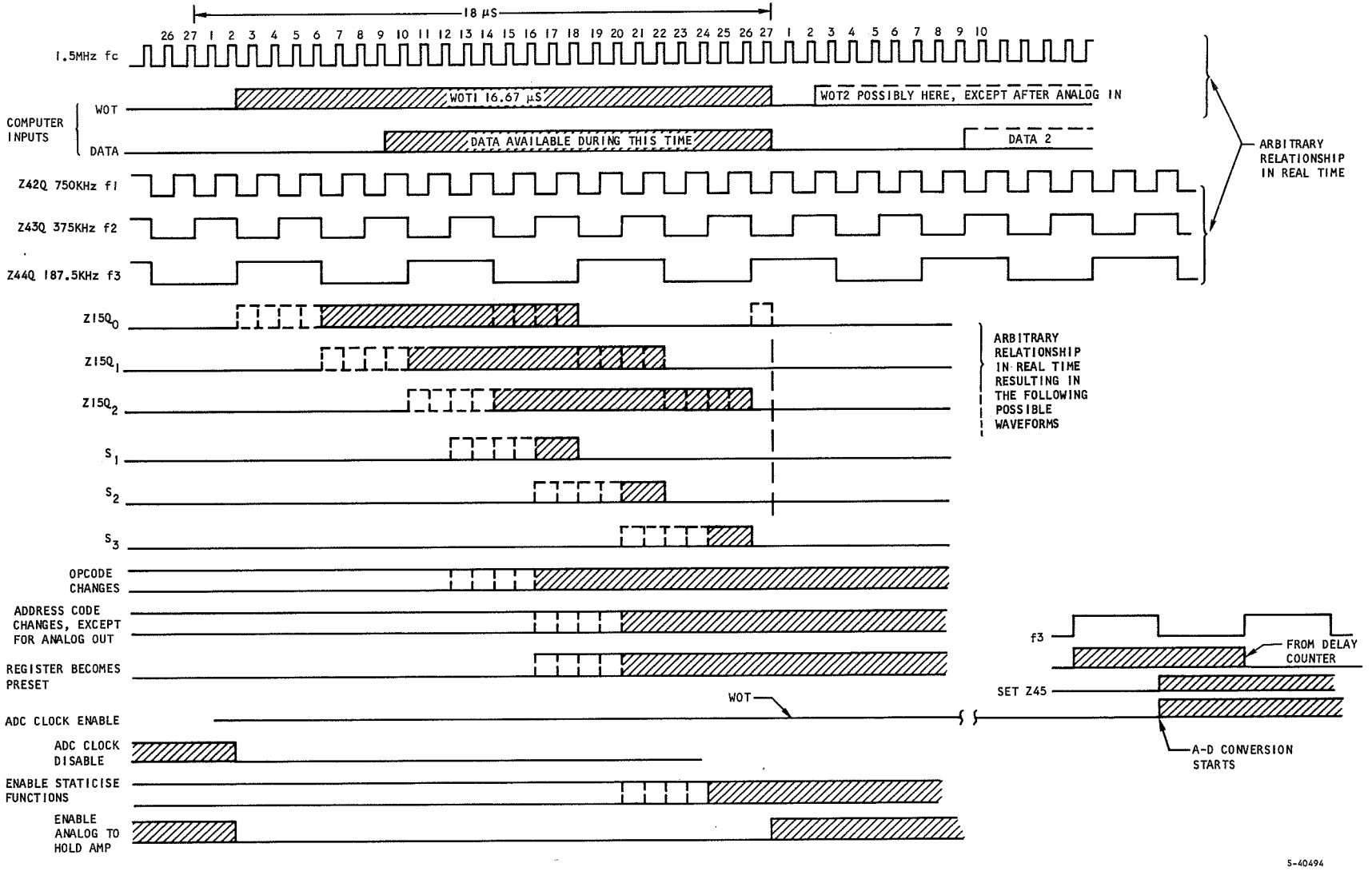


Figure 6.3-3. Interfacing Timing

6.3.1.3.2 Computer Instruction Detector and Transfer Control Sequencer

The status of the WOT line is shifted through a shift register, Z15, except when the WOT is FALSE, by clock f_2. As soon as the WOT is detected (by concurrence of WOT and f_2) $Z15Q_0$ becomes TRUE. This state is shifted through the shift register and $Z15Q_1$ and Q_2 becomes TRUE. When Q_2 becomes TRUE, Q_0 is arranged to become FALSE regardless of the state of the WOT line. This state is shifted through the shift register.

Figure 6.3-3 shows that the WOT signal initiates the generation of three pulses, delayed with respect to each other by one f_2 clock period, at $Z15Q_0$, $Z15Q_1$ and $Z15Q_2$, respectively.

These three pulses and clock f_2 are gated together to produce the transfer control pulses S_1, S_2 and S_3 with a width and separation equal to clock f_1 period.

S_1, S_2, and S_3 establish the timing for sequencing, in synchronism with the CIU clocks, the interface data conversion, and transfer functions.

6.3.1.3.3 Operation Code Memory and Decoder, Transfer Control Signal Generator

The S_1, S_2, and S_3 pulses always occur during the period for which information is available at the computer interface. This information may be an instruction and/or output data (as defined in para. 6.3.1.2, Input/Output Instructions).

Bits 13, 14, and 15 contain the operation code (Opcode) which describes the transfer function to be performed by the CIU. This Opcode is loaded into a memory Z13, by the control term S_1, and decoded by the decoder Z14. Z14 produces one-out-of-ten enable signals which, in turn, select further controlling functions in the gate network Z24, Z25, Z32, Z33, and Z34. This gate network, together with the control terms S_2 and S_3, generate all of the fundamental transfer control signals required within the CIU. These signals are shown in Figure 6.3-3.

6.3.1.3.4 Computer Output Address Data/Bus

All of the signal lines from the computer interface are presented with a normalized load, in fact, a single standard gate input.

The output of each gate drives a bus which routes the address/data to the I/O transfer register, an address memory, and a discrete data output memory.

Each memory is loaded depending on the Opcode set up in the Opcode memory.

The address memory, Z9 and Z11, is always loaded with the status of the eight address/data lines except when the Opcode describes analog data output, in which case the address memory will have been previously loaded with the address of the analog output. The discrete-output memory cells are "set" or "reset" to the status of the eight address/data lines when the opcode describes "set-discrete" or "reset-discrete," respectively.

The I/O transfer register is set to the state of the eight address/data lines when the Opcode describes analog data output. The output of the interface DAC which produces the analog signal. The analog signal is then demultiplexed to the analog holding circuit described by the address (which will have been previously set up) in the address memory.

6.3.1.3.5 Address Memory and Decoder

The address memory, Z9 and Z11, is always set to the status of the eight address/data lines except when the Opcode memory has been loaded with the Opcode for analog data output.

The Opcode memory is staticized by the S_1 control term and the address memory by the S_2 control term.

When the computer address/data lines contain address data, the least significant six bits are decoded to produce an $8_{10} \times 8_{10}$ matrix by Z10 and Z12. The 16 (8+8) resulting signals are fed, via buffers, to the analog input multiplexer decoder, which produces the multiplexer drive signals.

Four states of the decoder Z10 are used to produce the drive signals for the demultiplexer which routes the DAC signals to the analog holding circuits.

Two states of the decoder are required to select one of the two sets of discrete inputs for the "discretes-in" Opcode.

6.3.1.3.6 Discrete Output Signal Memory

The discrete output signal memory retains the states of the eight discrete output signals. The eight memory cells can be individually set or reset by the appropriate Opcode (set output discretes or reset output discretes) and an 8-bit address. A signal bit is made TRUE in the address to select the cell which is to be switched. While this form of single-bit-address was chosen for simplified programming, all eight cells can be switched simultaneously with the appropriate address (i.e., all bits of the address TRUE).

6.3.1.3.7 ADC Start Conversion Delay Circuit

When an analog input is selected by the computer instruction, a period of approximately 50 μsec must be allowed for the multiplexer to switch and the appropriate signal conditioner to settle, before the analog-to-digital conversion can begin. This delay is generated by the counter Z16 and is initiated by the WOT signal changing from TRUE to FALSE.

The ADC is preset by the S_2 control term but will not begin a conversion until the (single) converter clock is enabled by setting Z45.

Z45 is set by clock f_3 when Z16 reaches the count 0111. The counter has a variable count facility, arranged by changing the number to which the counter is initially preset. The count period can be increased or decreased in increments of 5.3 μsec by changing the preset state.

As shown, the counter counts through nine states, clocked by f_3. Due to the manner in which the WOT instruction is recognized, and the phase of clock f_3 relative to clock f_2 when the control term S_2 is generated, the total delay between multiplexing an input and beginning the conversion varies.

The total access time for an analog input is determined as follows:

(a) Time to recognize instruction and generate multiplex-signals: 9.35 μsec to 12 μsec

(b) Conditioner settling delay period, which is 45.3 + (12 or 14.6) μsec i.e., 57.3 or 59.9 μsec

(c) ADC conversion time which is 50.7 for 10 bits (add or subtract 5.34 μsec/bit for more or less bits, respectively)

Therefore, minimum access time: 117.3 μsec; maximum access time: 122.3 μsec.

Once the counter has started it will continue to count through its complete counting sequence of 15 states until it is reset again by a WOT instruction. This will not, however, alter the required control terms associated with the setting of Z45, which enables the converter clock.

6.3.1.4 ADC Logic and I/O Transfer Register

The I/O transfer register is a multifunction register and is involved in analog inputs, storing of discrete inputs from two sources and storing computer outputs for digital-to-analog conversion. In an A-D mode the register, with associated gating, performs as a successive-approximation converter. In the remaining modes the register acts as a parallel entry memory.

The register is mechanized with master-slave flip-flops which have both synchronous and asynchronous data entry facilities. The synchronous R-S input facilities are used for the converter logic; the asynchronous inputs are used for parallel data entry. The circuit for this portion of the digital section of the interface is shown in Figure 6.3-4. The detailed operation is explained below; the two basic operating modes are identified as asynchronous input/output transfers, and A-D conversion.

6.3.1.4.1 Asynchronous Input/Output Transfers

Discrete data inputs and the computer digital data output form the asynchronous input/output transfer signals.

The data are entered into the register via data gates, one for each data source. The outputs of the data gates are wire-or connected on a bit-for-bit basis. Each wired function is connected to the asynchronous input of the associated register cell. To enter these data, the register is first preset (cleared); then the chosen data gate is momentarily enabled allowing the data at the input to the data gate to enter the register. The clock to the register is inhibited during this process, so the contents of the register will remain unchanged when the data gate is again inhibited.

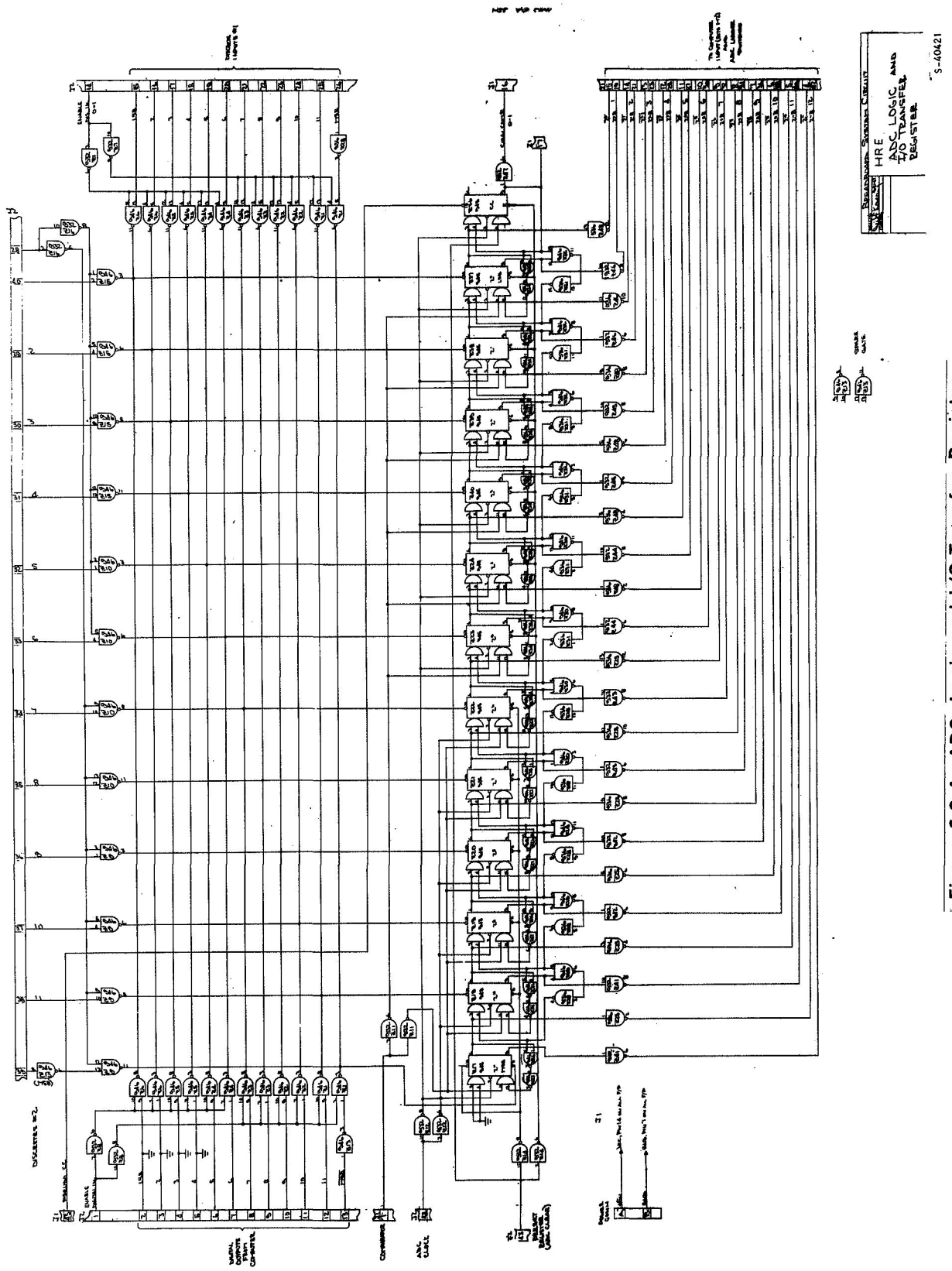


Figure 6.3-4. ADC Logic and I/O Transfer Register.

Three sources of data are shown in Figure 6.3-4: two sets of discretes and the computer output. When the computer instruction requires discrete data input, the interface control logic will issue the necessary signals to preset the register and "enable" the addressed data gate. The computer will then interrogate the contents of the register.

When the computer instruction requires the register to load the computer parallel output data, the same procedure is followed, but the appropriate data gate is used. In this case the register output, which is connected to the DAC, is not interrogated. Instead, the output of the DAC is demultiplexed to the addressed holding circuit, which in turn controls an actuator.

The DAC always follows the contents of the register, regardless of the operating mode. However, since the output of the DAC is only used for A-D conversion and D-A conversion, its value is only important when these operating modes are selected; in such a case the register is loaded with the appropriate number.

Figure 6.3-4 shows that when the register is preset all stages are "cleared" except the most significant bit (MSB) Z17, which is "set." In the A-D operating mode, in which the register forms part of a successive approximation converter, time is saved by having the MSB set when the conversion begins (DAC output is mid-scale). Consequently, for discrete and digital data entry the data bit in the MSB position of each data gate is inverted to compensate for the "set" condition of the most significant register bit.

6.3.1.4.2 Analog-to-Digital

Only the synchronous inputs are used in the analog-to-digital conversion operating mode. The register is preset initially to a number (MSB TRUE, all other bits FALSE) which produces half-scale output at the DAC connected to the converter.

By successive-approximation method of conversion, the digital equivalent of an analog signal is arrived at by trial and error. This involves successive approximation of the analog signal, with progressively less significance as the conversion proceeds.

This technique is inherently faster than an integrating technique, and the conversion is completed in a fixed time period, regardless of the value of the analog signal.

The conversion starts by comparison of the mid scale output of the DAC and the analog input. The comparator output (not shown in this section of the interface) will indicate whether the input is greater or less than midscale. The MSB of the converter is left set if the input is greater than midscale, and is cleared if the input is less than midscale. The converter now adds one-quarter scale to the DAC output by setting Z18, the (MSB-1). Again, the comparator indicates the quarter of the scale in which the input belongs; the MSB-1 is switched accordingly.

This process is repeated until the least significant bit (LSB) is decided, at which point the conversion is complete.

The use of master-slave register elements requires a single clock signal to perform the conversion.

The conversion process is best illustrated with respect to Figures 6.3-4, 6.3-5, and 6.3-6.

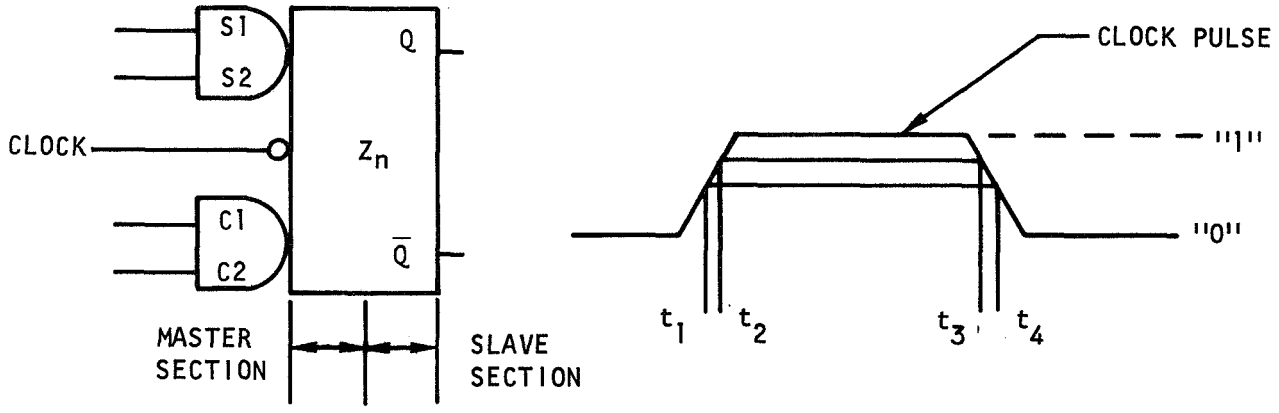


Figure 6.3-5. Master-Slave Flip-Flop

Figure 6.3-5 shows a flip-flop of the type used in the ADC. The points defined by f_1, f_2, f_3, and f_4 of the clock pulse have the following significance relative to the switching action of the flip-flop:

f_1: Inhibit the slave section (output)

f_2: Enable the master section (input)

f_3: Inhibit the master section (input)

f_4: Enable the slave section (output)

This means that data is entered into the flip-flop between the times f_2 and f_3, and the output assumes the state of input of f_4. This two-phase operation allows data to be transferred between adjacent stages (serial shift mode) of the ADC register reliably without race problems due to differing propagation delays of elements.

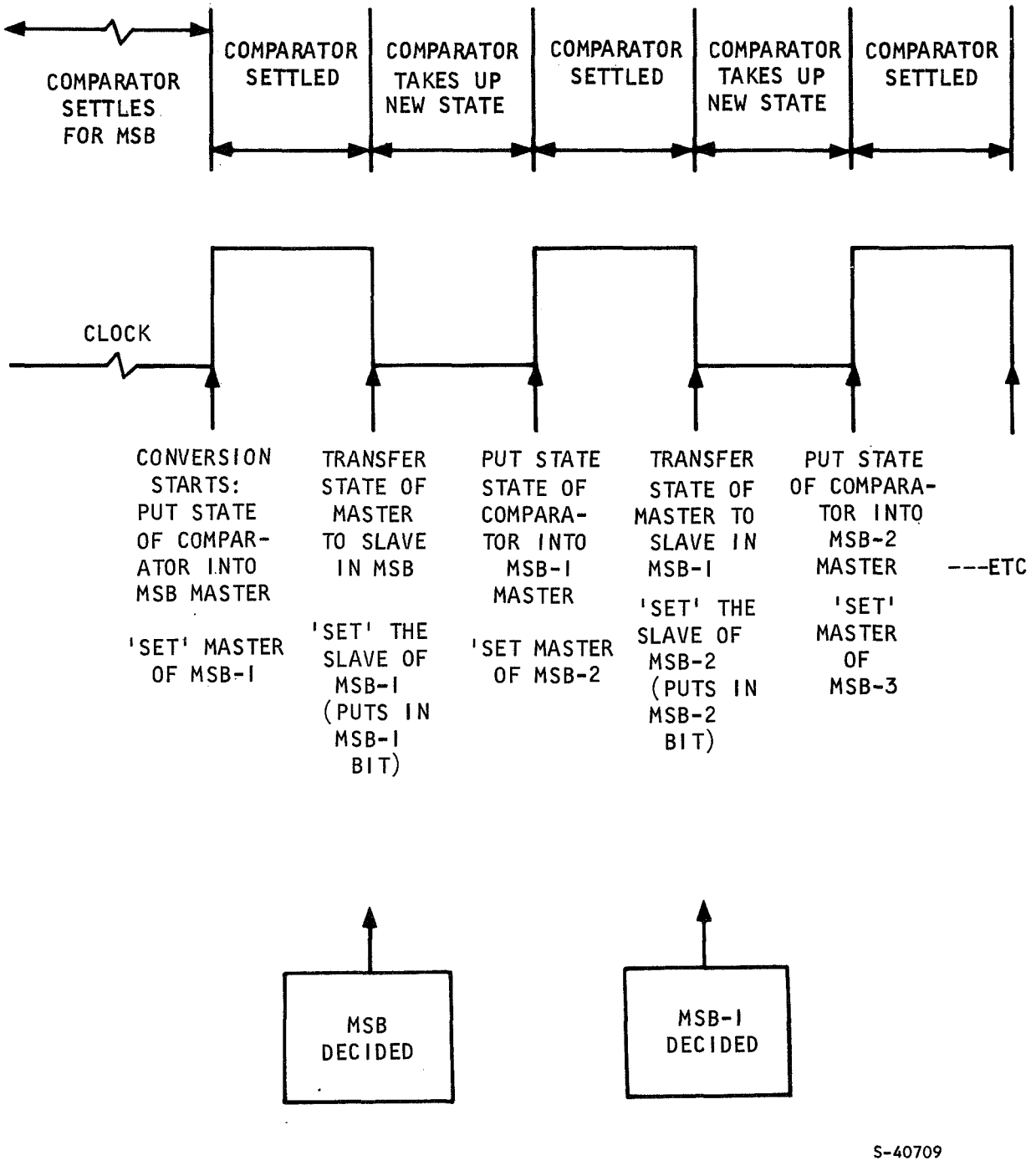


Figure 6.3-6. Analog-to Digital Conversion Process

The significance of this facility is that the converter can be mechanized using the existing I/O transfer register, together with a number of gates which generate the set and clear terms for each stage.

Referring to Figure 6.3-4, each register stage is connected to a clock via the buffers Z12. The state of the comparator is fed to all stages via the buffers Z11, and the register is preset via the buffers Z14.

A "carry" signal is generated by the logical AND of the register elements, using gates Z26, Z27, Z33, Z34, and Z35. The carry signal ensures that as each stage is "decided" it will remain unchanged during subsequent stage decisions.

The conversion process relative to the clock is shown in Figure 6.3-6.

Ten clock pulses are required for complete conversion; the time taken for conversion equals 9.5 clock periods, or 50.7 μsec.

6.3.1.4.3 Multiplexer Decoder

The multiplexer decoder shown in Figure 6.3-7 can select up to 64 channels, though only approximately 40 are allocated at present. Each channel is selected from an 8 x 8 matrix by choosing the position on each axis with two one-out-of eight decoders fed by a split 6-bit binary code.

Since several conditioners are involved in signal multiplexing it is necessary to multiplex not only input signals, but also conditioner output signals. This is done by a postmultiplexer driven by the most significant half of the 6-bit address code.

Thus, the most significant 8-position decoder within the interface control logic (Z11) drives the postmultiplexer, and the logical AND of one-out-of-the-eight signals of both the most significant and least significant decoders (Z11 and Z9) forms the drive signal to each of the input signal switches of the multiplexer.

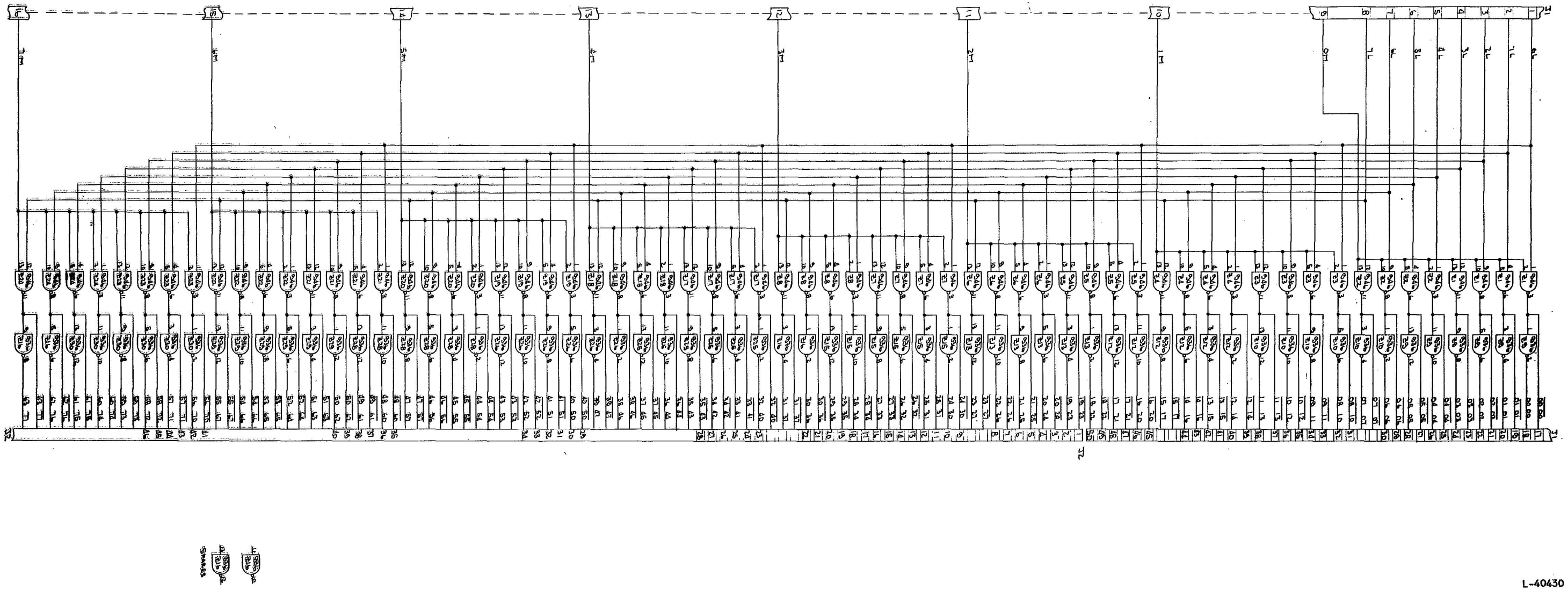
For breadboard purposes the multiplexer decoder generates normal and inverted signals. The final system will be tailored to suit the exact switching requirements when the signal list is finalized.

6.3.1.5 Function Interconnections

The interconnections between the three major sections of the digital portion of the interface are shown in Figure 6.3-8.

6.3.1.6 Teletype Interface

Initially, it is intended to connect the control system and the computer ground support equipment (GSE) to the computer to provide greater monitoring and display facilities than would otherwise be available. Further, with this arrangement it will be possible to take advantage of the teletype interface within the GSE.



L-40430

Figure 6.3-7 Multiplexer Decoder

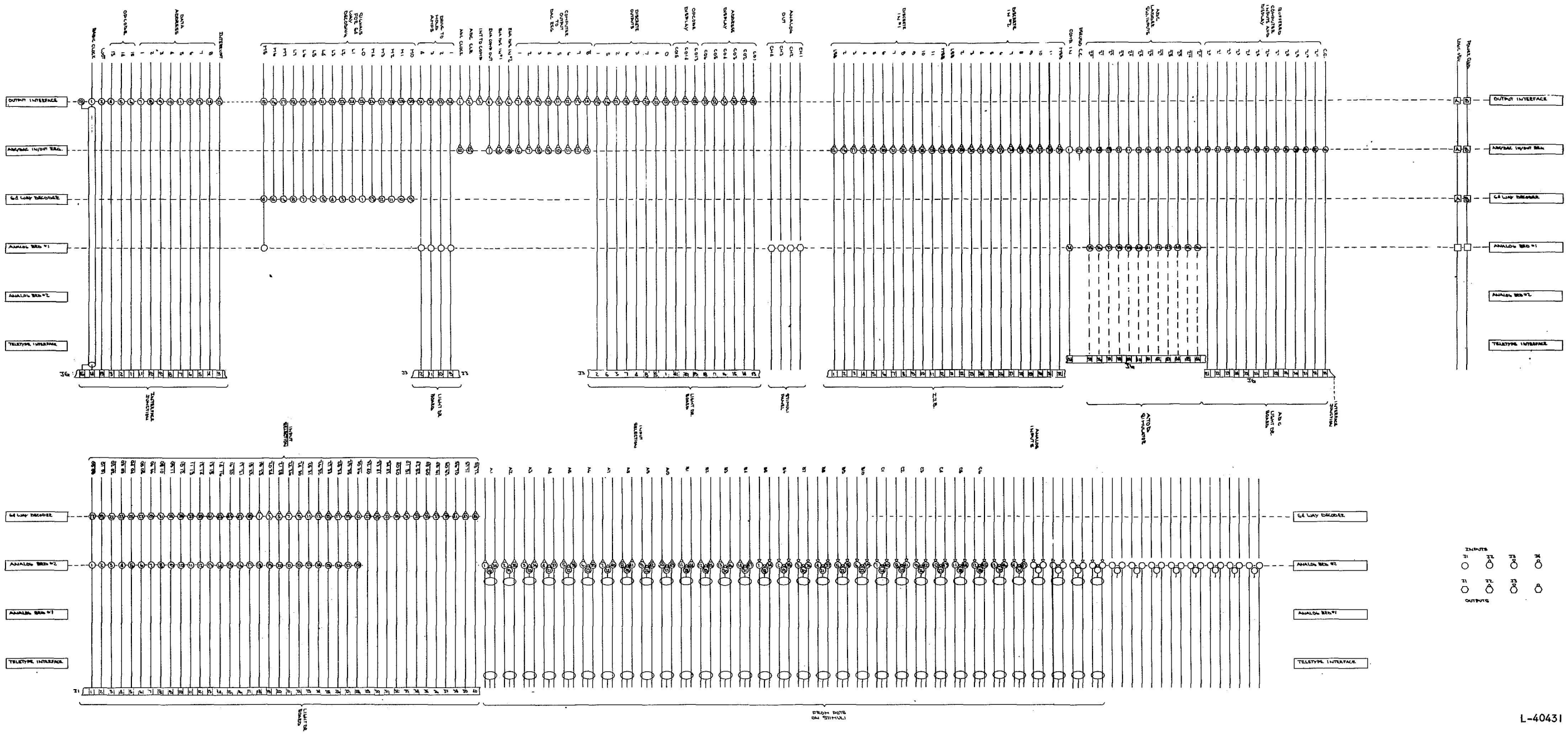


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Figure 6.3-8 Function Interconnections

A teletype interface will be included in the control system in its final form, and this interface is currently undergoing detailed definition and design. Most of the existing facilities within the digital portion of the interface can be used to create a parallel input/output interface between the computer and the teletype unit.

Additional hardware will amount to an assembler register with associated control logic for assembling teletype input and output words. One of the spare computer instructions will be used to transfer data from the computer via the interface to the teletype for printer/punch. The computer interrupt capability will be used to prepare the computer for accepting data from the teletype keyboard/reader.

6.3.1.7 Auxiliary Communications

Though further interfacing with the computer is not defined at present, a complete record of all communications within the computer-controlled engine control system could be derived by monitoring the computer output bus and input bus.

This would allow a real-time assessment via telemetry, of system performance as a whole, and, in the event of a malfunction, a timely correction shutdown could be possible.

If recordings are made, the data could be used to analyze engine and control system performance in detail.

The asynchronous nature of the control system and likely recording and/or telemetering facilities necessitates engineering of appropriate control logic to ensure correct transfer of data.

6.3.1.8 Monitoring

A gross check of the status of the interface is made by connecting the four analog outputs back into four analog inputs, and one bit of the discrete output back into one bit of each of the two discrete inputs. This enables the computer to check all of the basic I/O functions; it is not possible to check all signal paths for discrete inputs/outputs.

Critical discretes could be dealt with by triplication and majority logic voting. This technique has not yet been pursued as the total monitoring requirement is not fully established. Further system definition and operation will lead to a rigorous analysis of failure modes and effects, and the appropriate monitoring techniques.

The computer operation will be checked by a test routine which will output a go/no-go signal. A regular go signal from the computer will be detected by a functionally redundant monitor and will control shutdown. A gross check on the interface by the computer will be included in the test routine.

6.3.2 Fuel Control System Concept

Figure 6.3-9 shows the system in block form. Various sensor signals are low-level-multiplexed, conditioned to a 0- to +5-v range and high-level-multiplexed into a comparator; error feedback signal from the comparator performs a successive approximation of the input signal. Low-level multiplexing is utilized in the pressure transducer and thermocouple channels to minimize hardware.

The analog signal will be converted into a 10-bit digital signal of 5.34 μsec/bit. Total conversion time is 50.7 μsec. Settling time at the start of each 10-bit conversion is 57.3-59.9 μsec. Time to recognize computer instruction and generate multiplex switching is 9.35 →12 μsec. Total access time for a 10-bit signal is 117.3 →122.3 μsec.

The analog output information is multiplexed from the ladder network through a buffer amplifier to a hold amplifier and driver where the information is appropriately scaled to the required current levels in order to drive the valve loads. A minimum updating rate of 5 samples/sec into each hold circuit is required, with a time of 1 ms allotted for signal settling.

The pressure sensor signal channels are arranged so that 14 sensors are driven from a common excitation supply (10 v) and each sensor produces approximately 30 mv full-scale signal. The signal conditioning amplifier is referenced to ground to avoid common mode voltage problems from the pressure sensor bridge. As the 14 pressure sensors are common at two points, the outputs require double-pole multiplex switches into the signal conditioning amplifier (if bridges are connected at three common points there would be severe interaction between bridges).

Two such low-level multiplexers and signal conditioners are required to accommodate the total of 28 pressure sensors.

The LVDT channel is used to sense linear displacement of the spike. The LVDT is similar to a transformer having one stationary winding excited. Two windings (wound in opposite phase) are mechanically attached to the body whose displacement is to be sensed. Displacement of the core from the null position produces a voltage which is either in phase or out of phase with the excitation and whose amplitude is proportional to the displacement.

The LVDT is excited by an amplitude-controlled oscillator at 4-KHz, 5-v peak. The scale factor of the LVDT is 0.26 v/v/in. displacement (full range is ±2.75 in.). The LVDT output is sensed by a buffer amplifier, then demodulated, filtered, and bias-shifted to produce a voltage range of approximately 0 to +5 vdc corresponding to ±2.75-in. displacement.

The voltage corresponding to ram position is fed back to the spike hold amplifier and driver for control purposes. This signal is also high-level-multiplexed to the digital computer for monitoring purposes.

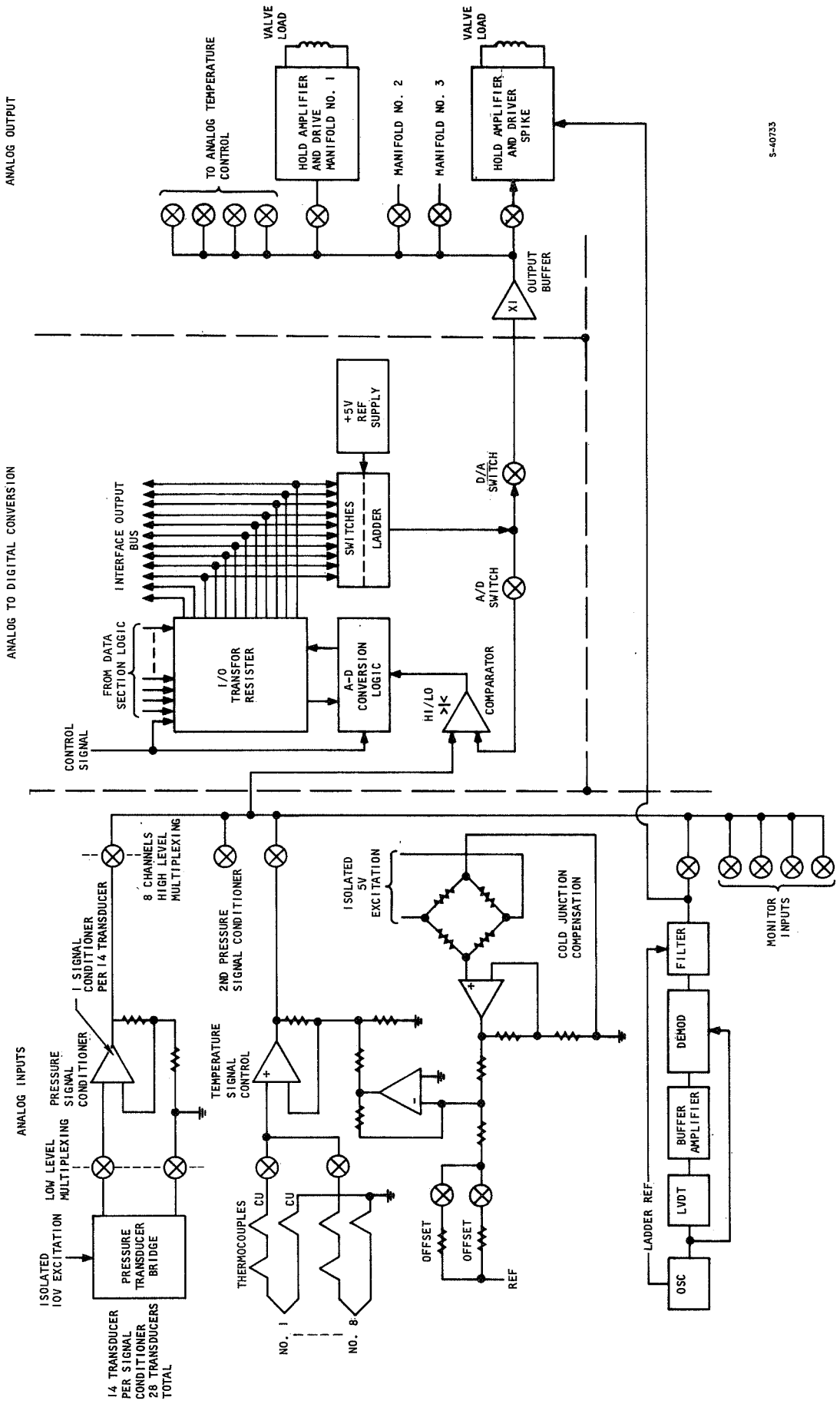


Figure 6.3-9. Fuel Control Interface, Block Diagram

The thermocouple channel multiplexes the different thermocouple offsets to cut down on hardware. The temperature signal conditioner will condition the full-scale temperature range to 0-5 v. A cold junction compensation bridge fed by an isolated 5-v excitation supply and will temperature-compensate the hot junction thermocouple. The thermocouple channel mechanization and design up to the high-level multiplexing will follow the analog temperature control mechanization and circuit design described in para. 6.4.

Appendix E contains a compilation of data sheets for the various integrated circuit devices used in the circuit descriptions of para. 6.3.2.

6.3.2.1 Analog Pressure Input Signal Conditioner Amplifier (Pressure Sensor) (see Figure 6.3-10)

This amplifier is noninverting and is arranged in three sections. Closed-loop gain is $1 + \frac{R15}{R14} = 149$.

Z_1 is a temperature-stabilized differential stage whose collector load is R_4 through R_8. Typical gain for this section is 34 db.

Q_1 provides a constant current source to bias the collectors of the differential stage Z_1 to 16 μA. This current will cause approximately +4 v drop across the collectors.

Q_2 is an emitter follower buffer stage used to avoid the input bias current drift of Z_2 being reflected to Z_1 input.

Z_2 provides a voltage gain of 92 db nominal. R_{15} and R_{14} are the closed-loop gain determining elements and are matched for scaling and temperature coefficient.

Provision is made at R_6 and R_7 for zero effect trimming of the amplifier. Frequency compensation of the amplifier is achieved by R_{11} C_1, R_{16} C_2, R_{15} C_5.

Typically, the closed-loop bandwidth is 200 KHz and may vary from approximately 70 KHz to 500 KHz corresponding to minimum and maximum open-loop gains of 114 db to 136 db.

Amplifier settling time is a function of both the slew rate of Z_2 and the closed-loop bandwidth, and is designed typically as 25 μsec to less than 0.1 percent full-scale signal.

6.3.2.2 Multiplexing

6.3.2.2-1 Low-Level Multiplexer (Figure 6.3-11)

Each switch consists of a double-pole single-throw switch mechanized with siliconix M103 MOS FET's (Q_1 and Q_2). Each switch requires a driver (siliconix D123F) and a gate (DTL 936) for logic interfacing.

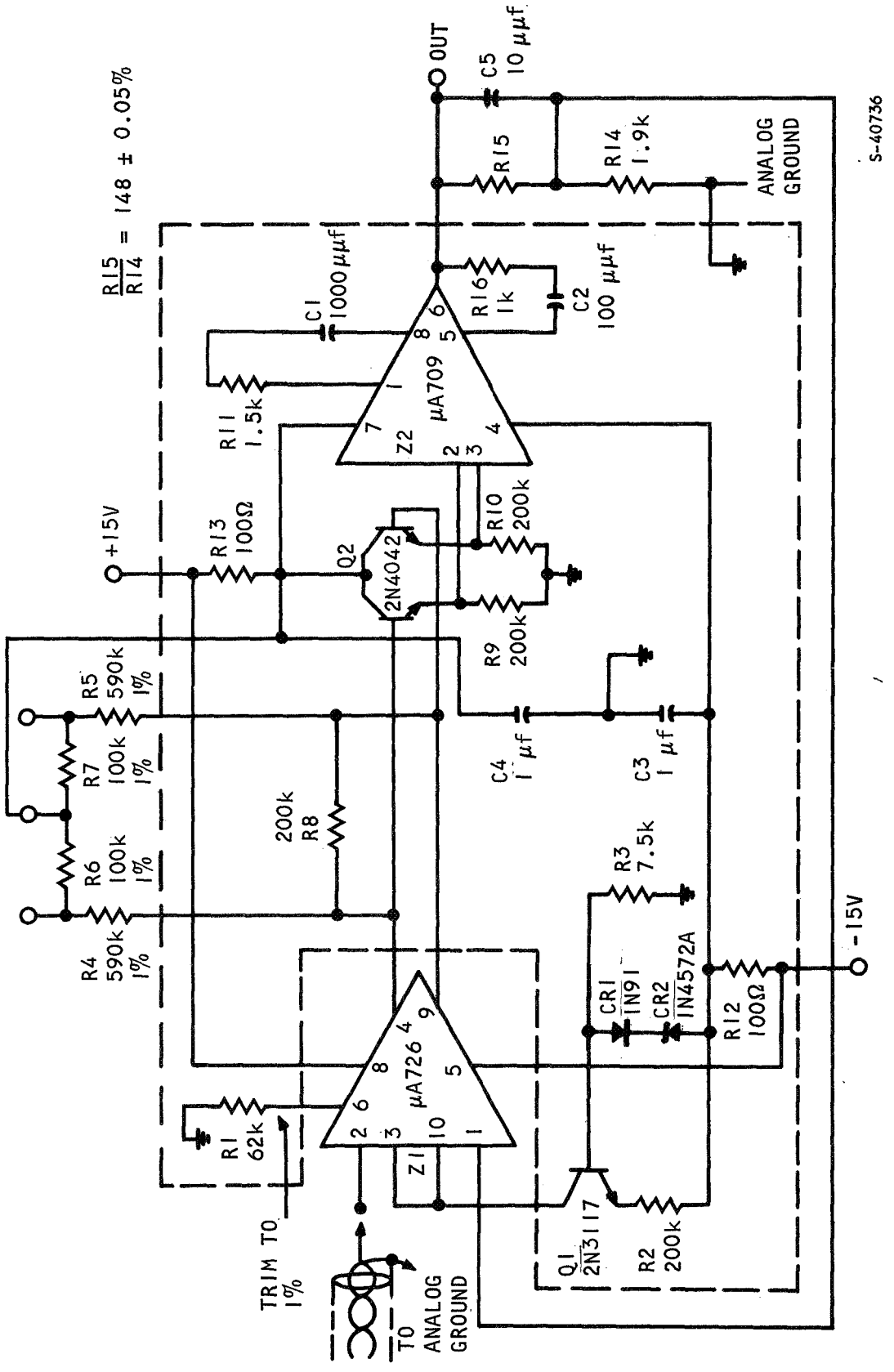


Figure 6.3-10. Pressure Transducer, Signal Condition (Thin Film)

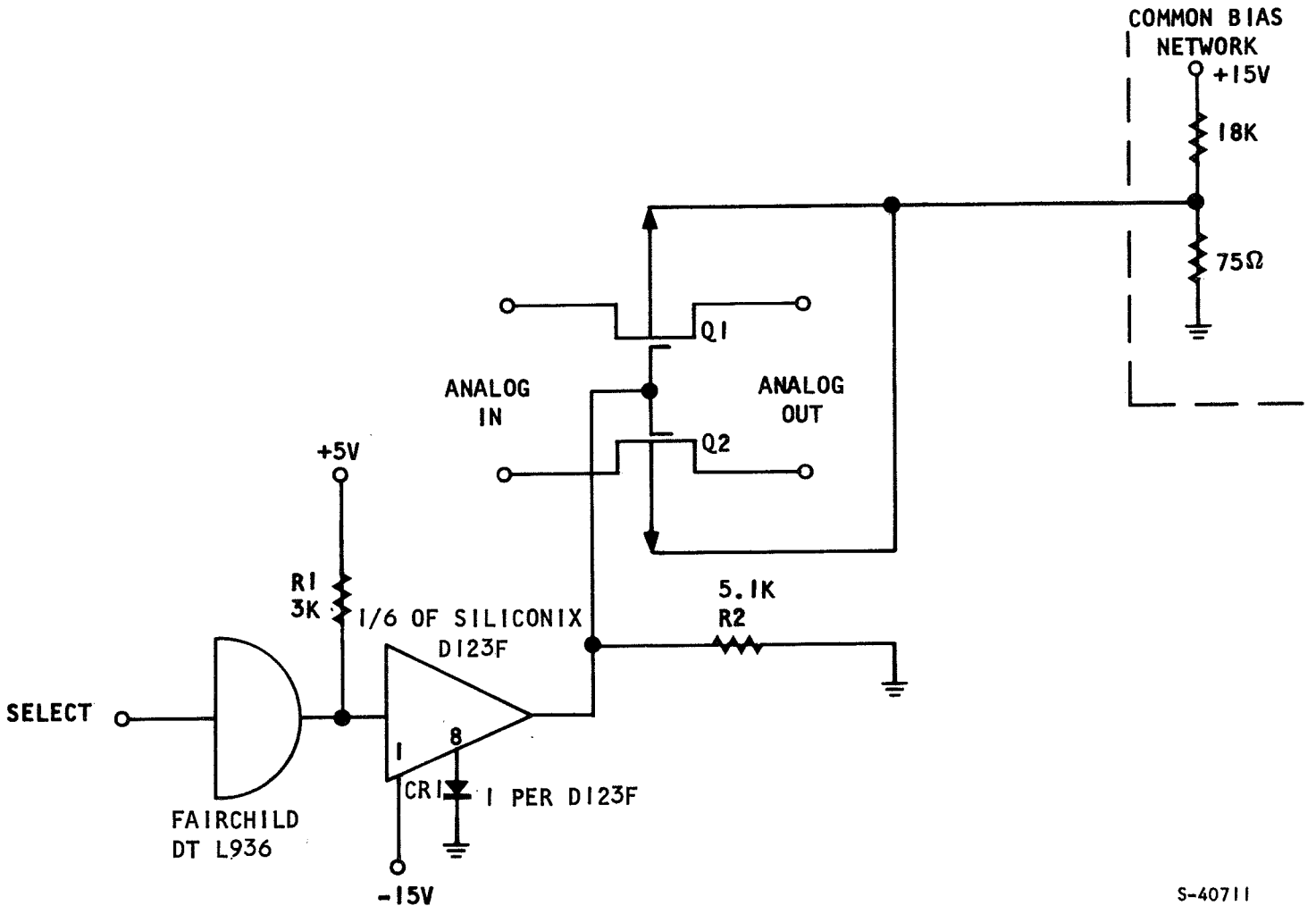


Figure 6.3-11. Double-Pole Switch - Typical (Low-Level Multiplexer)

R_1 is a pullup required to provide the necessary drive to the DI23F. R_2 turns off Q_1 and Q_2. CR_1 enhances the noise rejection of the DI23F.

Since the maximum analog signal input could be as much as 50 mv above ground when the channel off, the body of each MOS is biased at +50 mv (increased bias voltage would unnecessarily increase leakage current of Q_1 and Q_2).

Switching speeds of less than 1 μsec are obtained.

6.3.2.2-2 High-Level Multiplexer (Figures 6.3-12, 6.3-13, 6.3-14)

This multiplexer switches signals on the order of 5 v full scale from the input conditioners to the comparator. Two channels are also used as D/A and A/D select switch. The elements selected (GII8F) provide sufficiently low leakage and low on-resistance (approximately 250 ohm).

Switching speeds less than 3 μsec are obtained. A high select-input turns the channel on. Since the select-input is driven from a DTL 936 gate, then the gate input must be low for this condition.

The GII8F uses a P channel enhancement mode. MOS FET's are zener diode protected.

6.3.2.2-3 Analog Output Multiplexer (Figure 6.3-13)

This consists of an FET Q_1 with a driver and a gate element for logic interfacing. With the select-input low, Q_1 is turned off. Select input high causes Q_1 to turn on. R_1 is required to provide sufficient drive current into the DI23F driver.

R_2 provides for turn-off of Q_1. CR_1 is added to enhance the noise rejection of the DI23F. Q_1 is a 2N4222 which provides low leakage at 125°C while providing a suitably low "ON-RESISTANCE" for settling of the analog signal into the analog output channel hold capacitor switching times of the multiplexer are much less than the output signal settling time allotted (1 ms).

6.3.2.3 LVDT Electronics

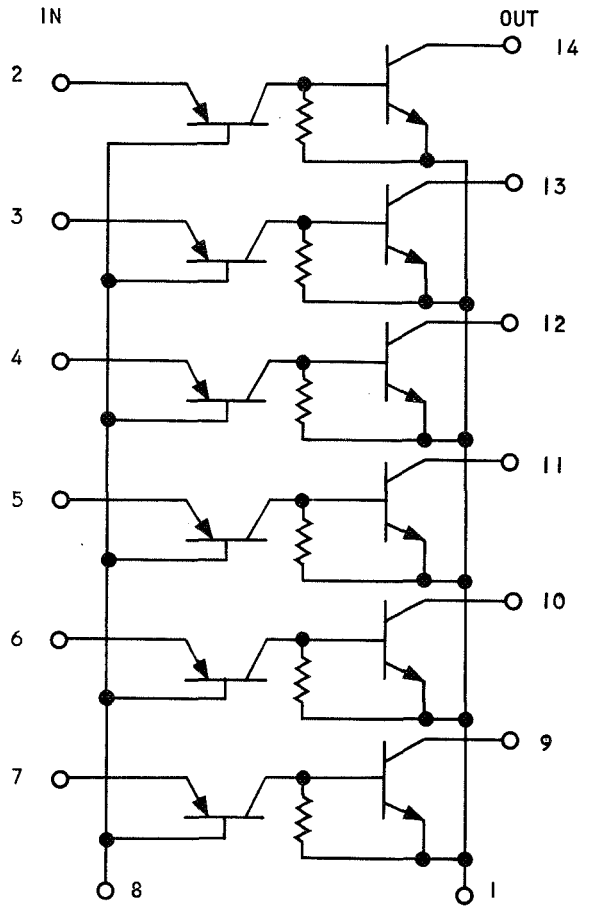
6.3.2.3-1 LVDT Oscillator (Figure 6.3-15)

The oscillator is a Wein-bridge type with the amplitude stabilized by means of an AGC loop. Amplifier Z_1 is mechanized as a noninverting buffer (with respect to input pin 2) and has it closed-loop gain determined by R_3, R_4, and R_{10} in parallel with the R_{on} of Q_7 which is the gain control element.

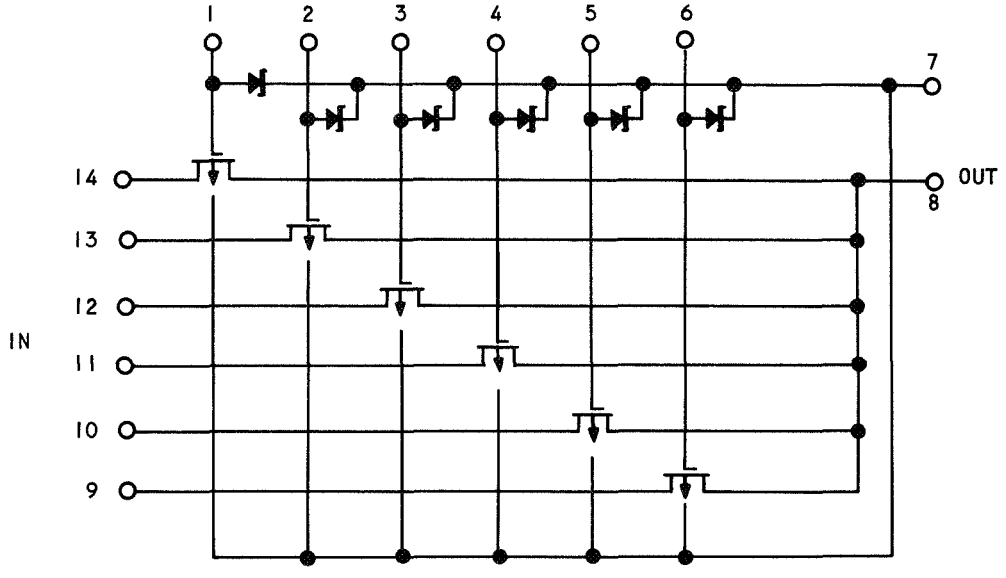
R_1, C_1, R_2, C_2 are the frequency determining components and for $R_1 C_1 = R_2 C_2$ the

$$f = \frac{1}{2\pi R_1 C_1} \text{ approximately (4KHz)}$$

SILICONIX D123F.



SILICONIX G118F.



S-40490

Figure 6.3-12. Siliconix D123F and Siliconix G118F

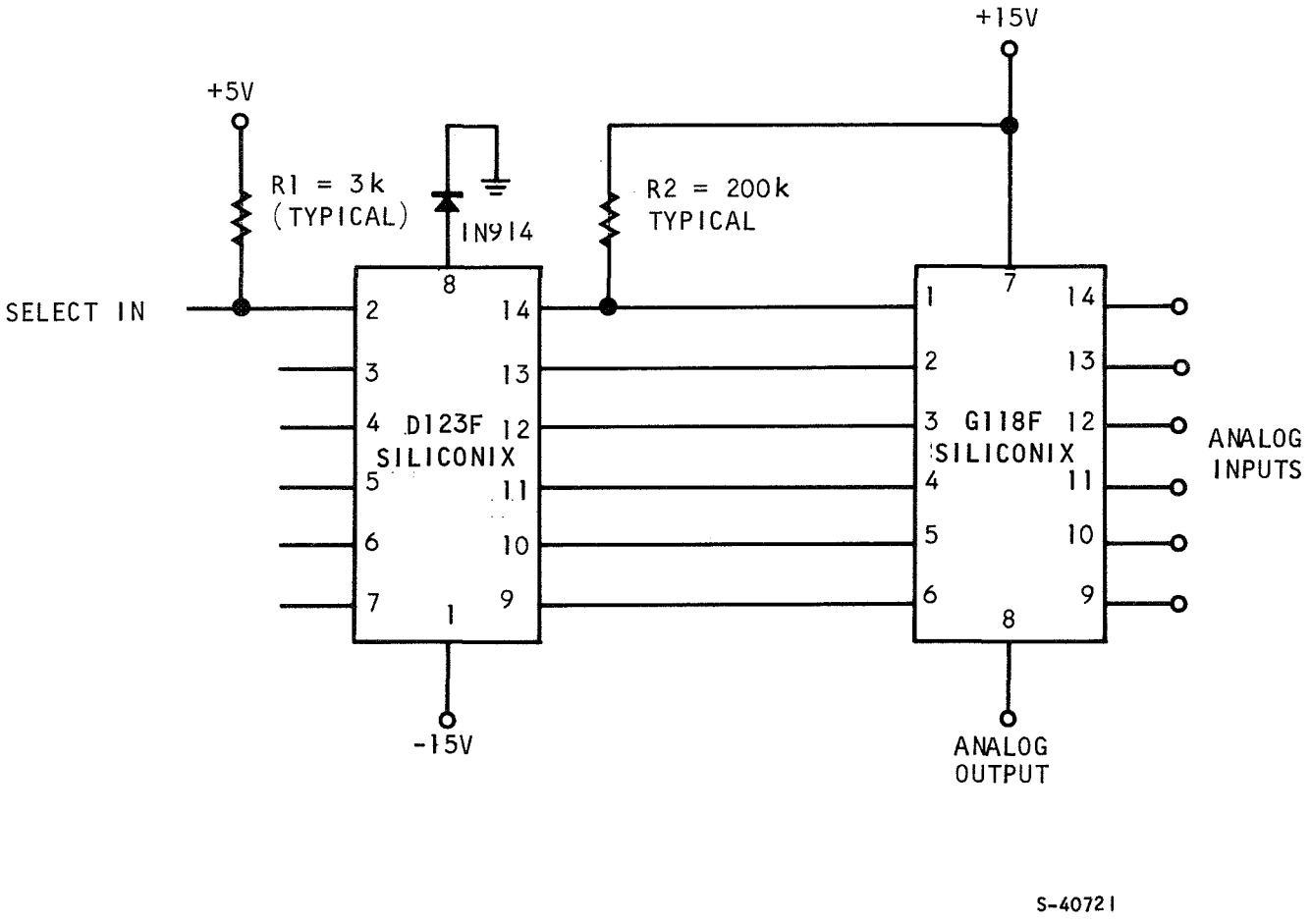


Figure 6.3-13. High-Level Multiplexer (Six-Channel Mechanization)

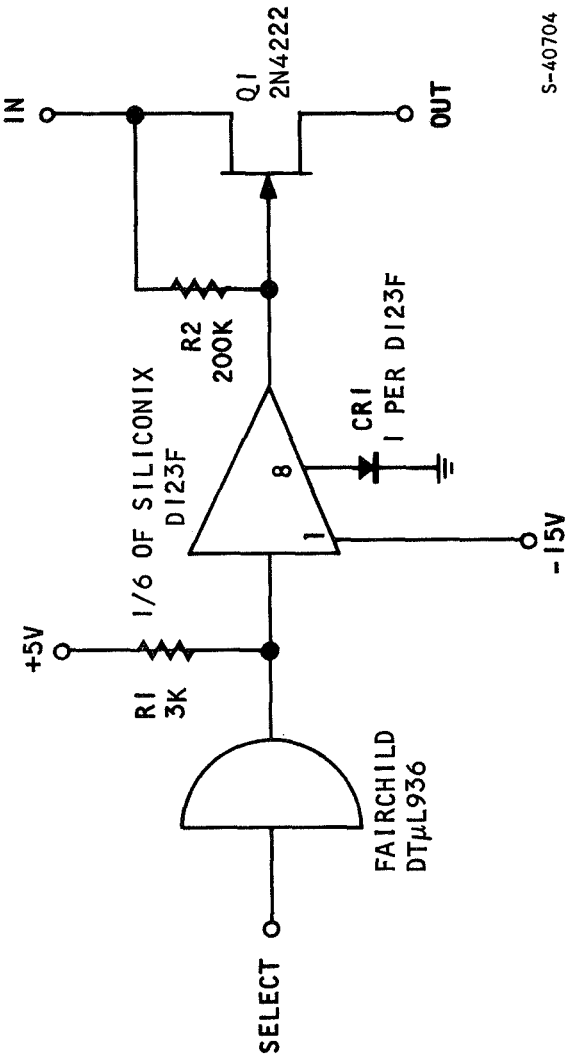


Figure 6.3-14. Analog Output Multiplexer (Typical, Single Channel)

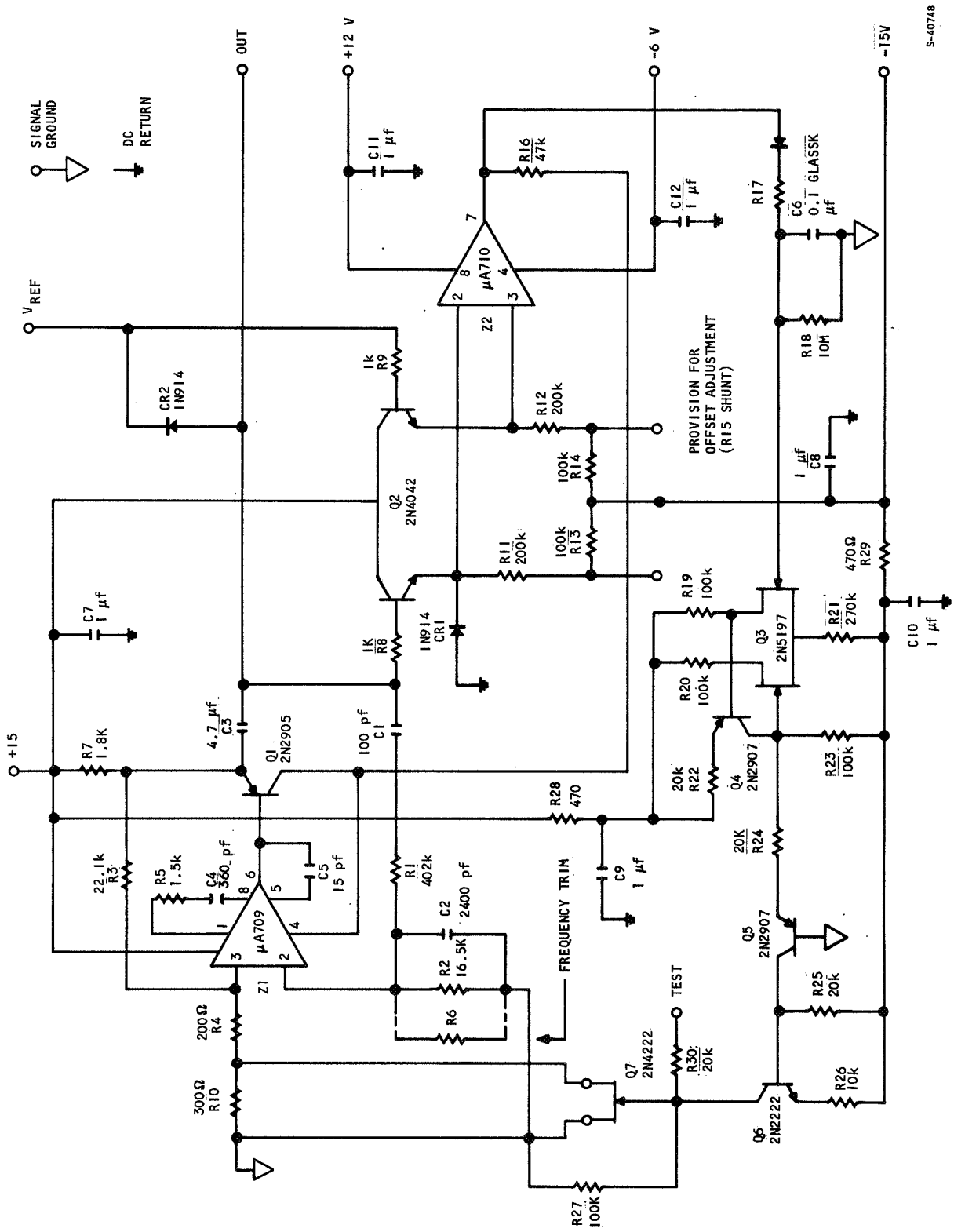


Figure 6.3-15. LVDT Oscillator

To sustain oscillation the closed-loop gain of Z_1 is

$$A > 1 + {}^{R_1}/_{R_2} + {}^{C_2}/_{C_1}$$

Q_1 is used as a buffer to provide current drive capability.

C_3 is used to ac couple to the output since the load (LVDT) is susceptible to dc and appreciable dc bias can exist at Q_1 emitter.

The oscillator output is maintained at a sinusoid peak value of V_{ref} (+5 v ladder reference supply) by means of the AGC loop.

The AGC loop has a comparator (Q_2, Z_2), a hold amplifier (C_6, Q_3, Q_4) and a level-shifting amplifier (Q_5 Q_6) with a control FET (Q_7).

Any increase in the peak output of the oscillator over the reference value is detected by the comparator which charges C_6. The control signal increasing (positive) at the input to Q_3 will produce a larger negative bias at the gate input to Q_7, thus increasing the R_{on} of Q_7. This, in turn, reduces the closed-loop gain of Z_1, thus forcing the amplitude of the oscillator to decrease.

6.3.2.3-2 LVDT Buffer Amplifier (Figure 6.3-16)

Since the LVDT output impedance is on the order of 500 ohms at 4 KHz and is variable over displacement of its core, its output must be sensed by a high-impedance amplifier. This amplifier is a conventional noninverting type with compensation to provide a loop gain of 66 db (nominal) at 4 KHz.

Since the output of the buffer amplifier is full-wave-rectified by a synchronous demodulator, no dc offset adjustment is required. Input peak sine wave is approximately ±3.57 v.

6.3.2.3-3 LVDT Demodulator (Figure 6.3-17)

This is a full-wave rectifier achieved by synchronously switching the amplifier Z_1 from a noninverting configuration (gain +1) to an inverting configuration (gain -1).

Noninverting condition:

$$V_{out} = V_{in}\left(1 + {}^{R_2}/_{R_1} - {}^{R_2}/_{R_1}\right) = V_{in}$$

Inverting condition:

$$V_{out} = -V_{in}\,{}^{R_2}/_{R_1} = -V_{in} \text{ as } R_2 = R_1$$

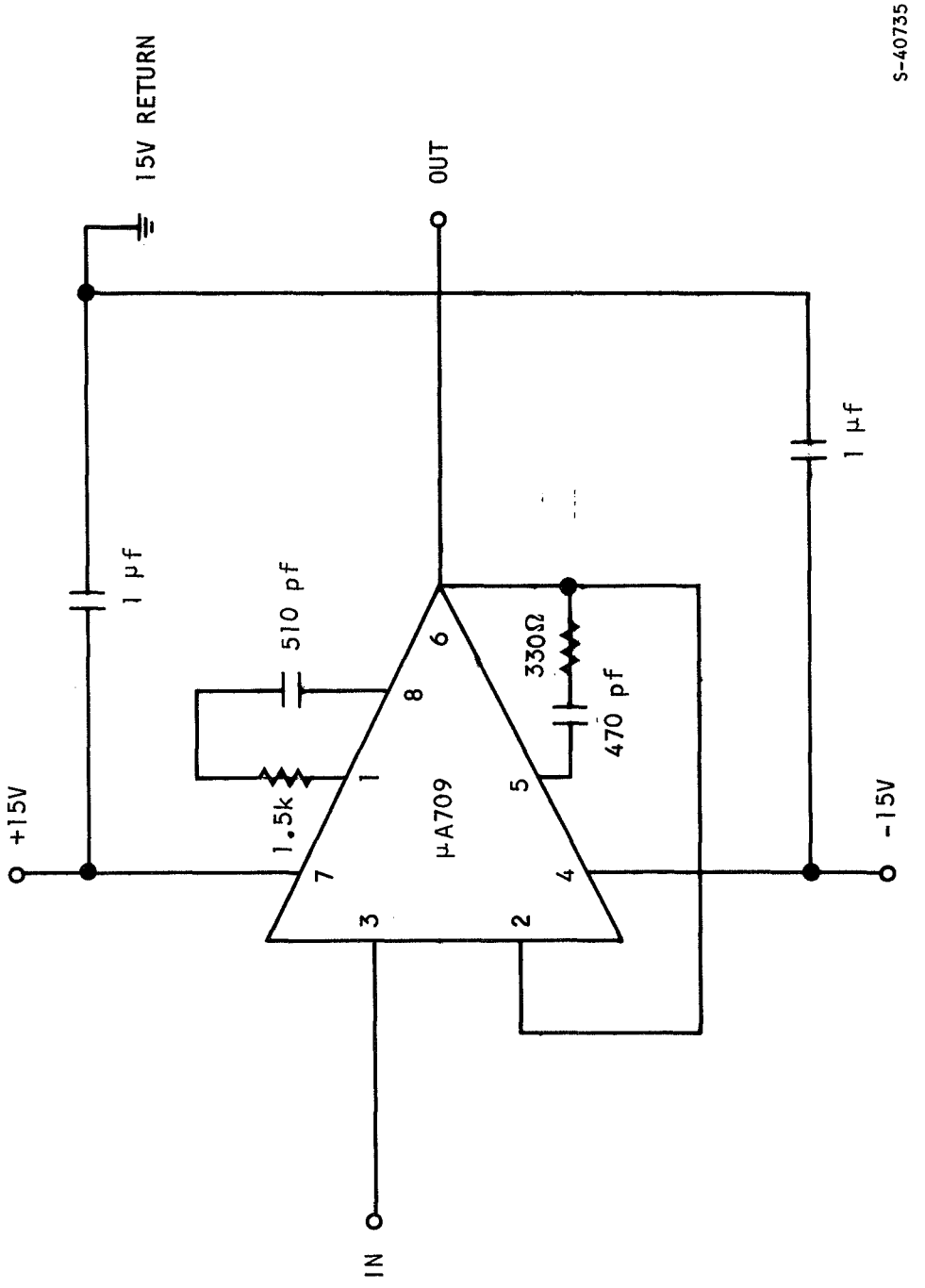


Figure 6.3-16. LVDT Buffer Amplifier

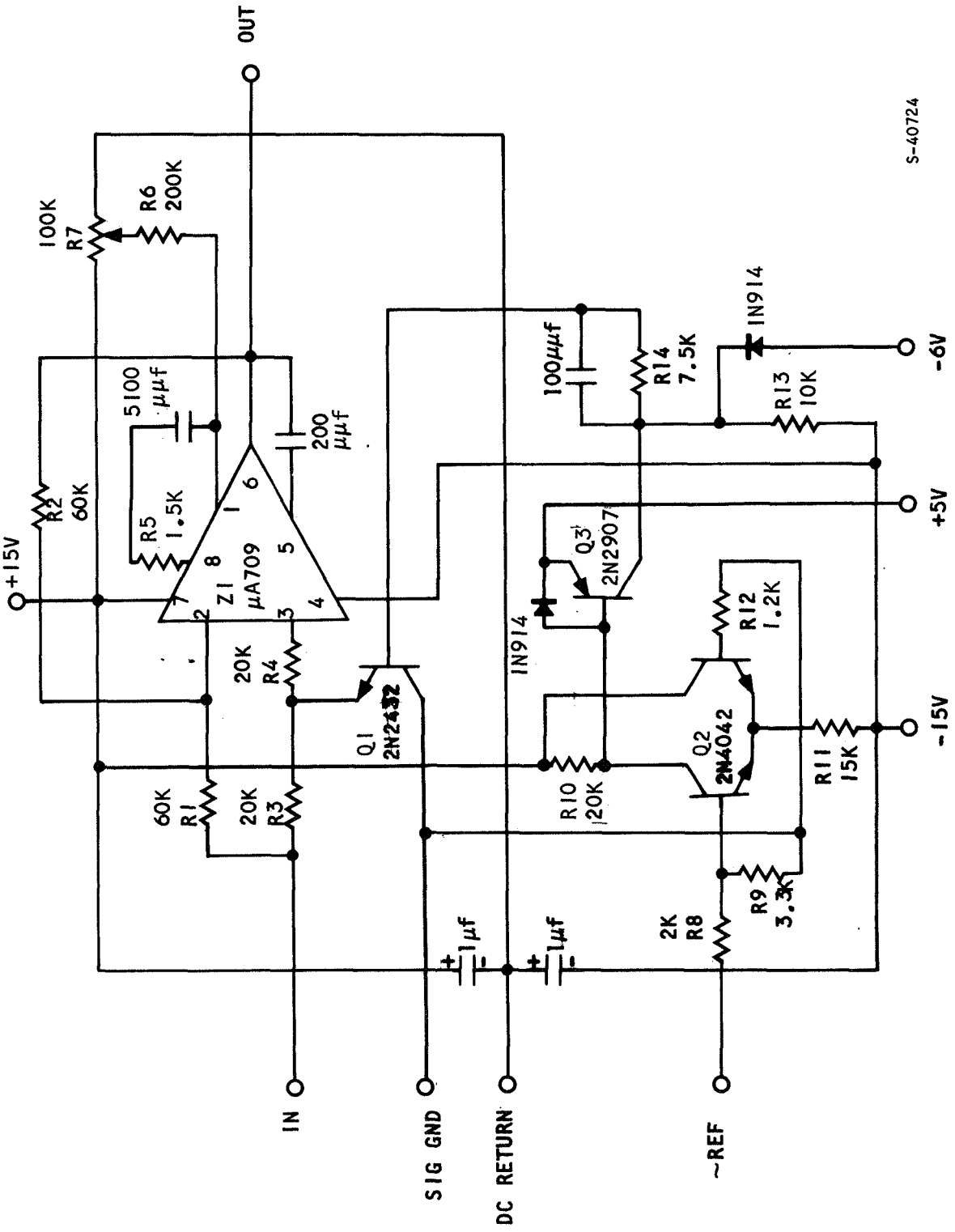


Figure 6.3-17. LVDT Demodulator

The gain configuration is controlled by chopper transistor Q_1 which switches R_3, R_4 to ground when the reference 4 KHz input waveform exceeds zero volts. Switching amplifier Q_2 Q_3 detects the zero volts crossover point. Initial dc offset of the demodulator is trimmed out by R_6, R_7. R_8 and R_9 are required to provide attenuation of the reference 4 KHz level (5 v) to prevent Q_2 from saturating.

6.3.2.3-4 Active Filter (Figure 6.3-18)

The input is full-wave-rectified, 1/2 sine waves at 4 KHz and of positive or negative polarity; the output is required to be dc in the range of 0 to +5 v. Therefore, a circuit performs the dual function of filtering and bias shifting.

$$V_{out} = -V_{in} \text{ (average value)} \frac{R_3}{R_1 + R_2} + V_{ref} \left(\frac{R_6}{R_5 + R_6}\right) \left(1 + \frac{R_3}{R_1 + R_2}\right)$$

for

$$R_3 = R_1 + R_2 \qquad \text{and} \qquad R_5 = 3\,R_6$$

$$V_{out} = -V_{in} \text{ (average value)} + \frac{V_{ref}}{2}$$

The filter is a 3-pole Butterworth with a cutoff frequency of 200 Hz since the first frequency component of ripple is at 8 KHz and the information frequency (modulation frequency of 4 KHz carrier associated with LVDT displacement signal) is in the 0 to 10 Hz range.

The transfer function of the filter is

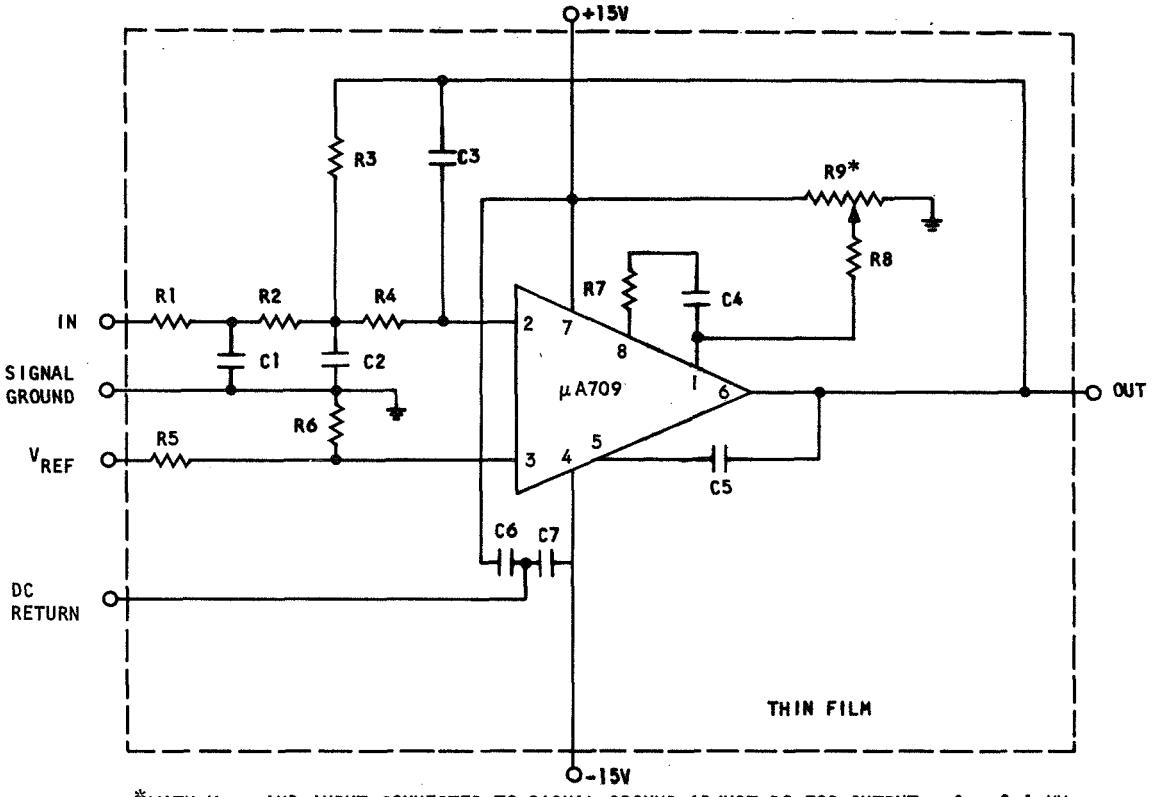
$$G(s) = \frac{-R_3}{A_s^3 + B_s^2 + C_s + D}$$

where

$$A = R_1 R_2 R_3 R_4 + C_1 C_2 C_3$$

$$B = C_3 \left[C_1 (R_1 R_2 R_4 + R_1 R_2 R_3 + R_1 R_3 R_4) + R_3 R_4 C_2 (R_1 + R_2) \right]$$

$$C = R_1 R_2 C_1 + C_3 (R_1 R_4 + R_1 R_3 + R_2 R_4 + R_3 R_4)$$



*WITH V_{REF} AND INPUT CONNECTED TO SIGNAL GROUND ADJUST R9 FOR OUTPUT = 0 ± 0.1 MV

C1 = 0.39 μf
C2 = 0.33 μf
C3 = 0.033 μf
C4 = 5100 μμf
C5 = 200 μμf
C6, C7 = 1 μf

R1, R2, R4 = 5k
R3 = 10k
R7 = 1.5k
R5 = 39.9k
R6 = 13.3k
R8 = 200k

R9 — TRIMMED OR SELECTED RESISTORS

S-40742

Figure 6.3-18. Active Filter

In this case $R_1 = R_2 = R_4 = R_3/2$

and C_1 C_2 C_3 are scaled to approximate the transfer function

$$G(s) = \frac{1}{(S + 1 = + S2 + S + 1)}$$

$$= \frac{-1}{(S + 1)(S + 1/2 + j^3/2)(S + 1/2 - j^3/2)}$$

R_8 and R_9 provide for dc offset trimming of the amplifier.

6.3.2.4 Analog Output

6.3.2.4-1 Ladder Output Buffer Amplifier (Figure 6.3-19)

This is a conventional noninverting unity gain amplifier with the addition of signal clamping at the input to avoid excessive signal levels appearing at the hold amplifier in the analog output channels.

Normal signal range into the buffer is 0 to approximately +2.5 v.

The clamping circuit at the input restricts the output to a range of approximately -0.8 v to +4 v.

Slew rate and bandwidth are not critical since the load has a specified setting time of 1 ms.

The drive capability must be on the order of ±3 ma at 0 to +2.5 v.

6.3.2.4-2 Manifold Fuel Valve Hold-Amplifier and Driver (Figure 6.3-20)

This circuit is arranged as a noninverting unity gain amplifier with the load connected inside the loop.

The voltage across R_1 will equal the input voltage, and consequently, the current in the load will be $\frac{V_{in}}{R_1}$.

This scheme provides an easy and efficient method of monitoring electronic failures, since the voltage across R_1 must match that value commanded by the computer (within specified limits) otherwise a no-go condition exists. Q_2 and Q_3 provide the necessary current gain, while the LM101 provides the necessary voltage gain. Q_1 and C_1 were selected to provide for a maximum signal droop of 1 percent for an update rate of 5 per second.

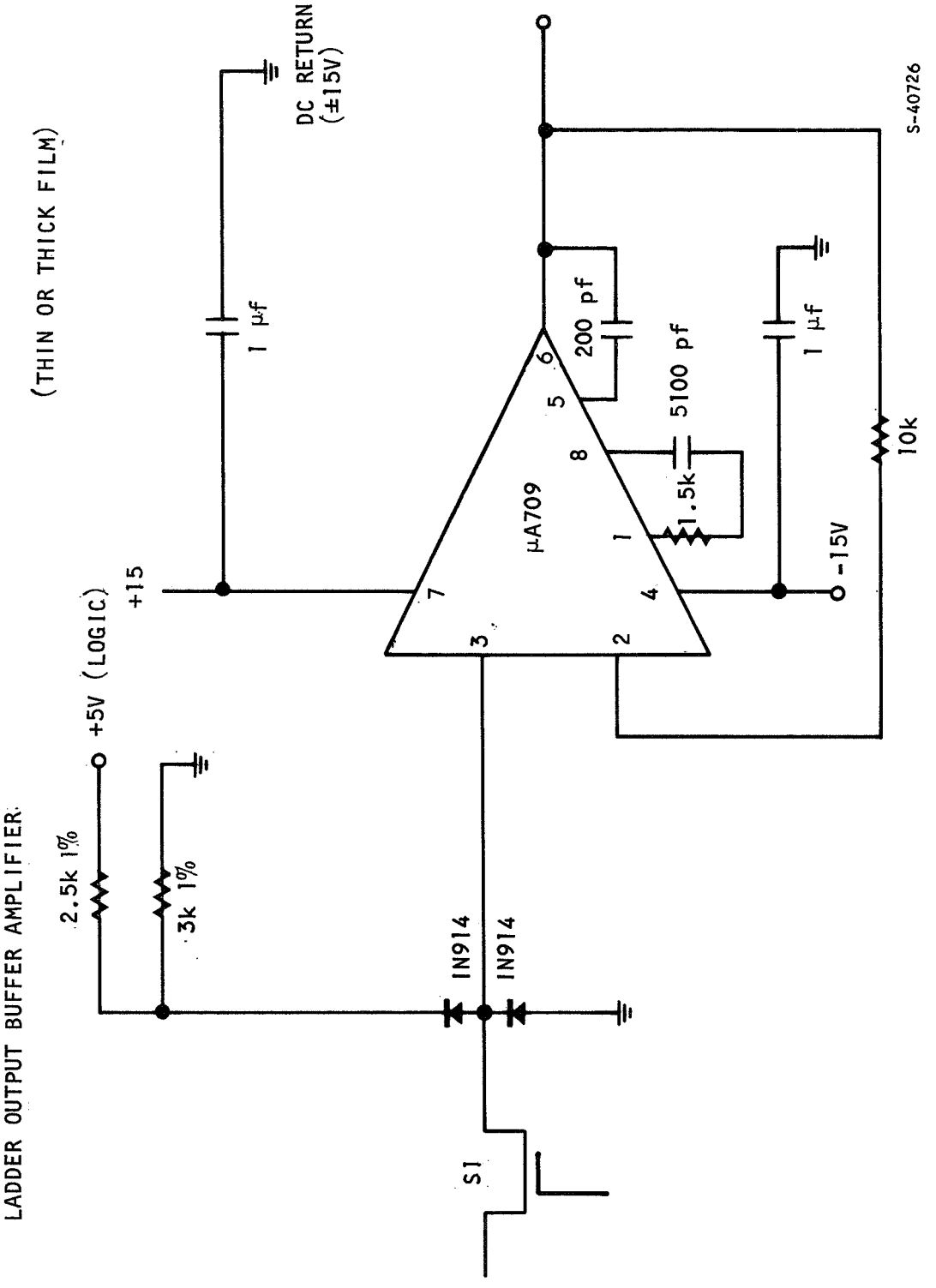


Figure 6.3-19. Ladder Output Buffer Amplifier

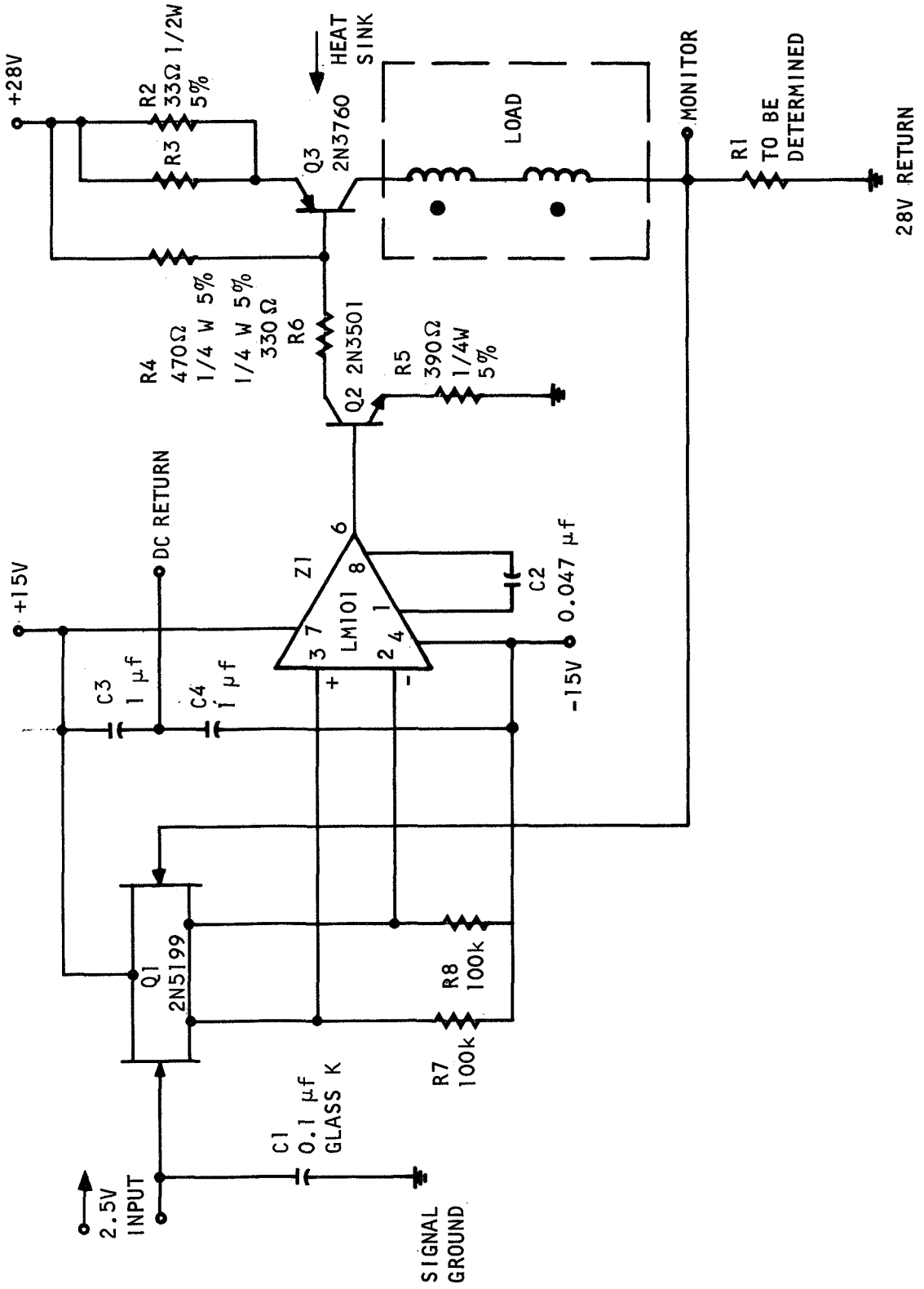


Figure 6.3-20. Manifold Fuel Valve Hold Amplifier and Driver

6.3.2.5 Analog-to-Digital Conversion

6.3.2.5-1 Comparator (Figure 6.3-21)

The comparator consists of an Amelco 807 BE operational amplifier with the input diodes clamped for differential input protection. The output is also clamped to produce approximately -0.6 and +5 v logic levels. Offset adjustment is provided by R_3.

Decision time for the comparator is approximately 3.5 μsec with input levels going from saturation to 5 mv of opposite polarity. Comparator speed depends on CR_3 CR_4 which serves to clamp the collectors of the first stage of the 807 BE, and C_1 which mechanizes the output section of the 807 BE as a Schmitt trigger.

Figures 6.3-22 and 6.3-23 show the comparator decision time.

6.3.2.5-2 Reference Supply (Figure 6.3-24)

Two temperature-compensated Zener diodes (CR_1 CR_2) and a resistor divider (R_3, R_4) are used to establish a reference voltage input to a unity gain non inverting amplifier Z_1 and Q_1.

Fine adjustment of the output is achieved by provision for offsetting Z_1.

Since the supply is required to primarily sink current from the ladder network, R_8 is used to preload the supply to accommodate this.

The response of the supply to step loads is shown in Figure 6.3-25 and 6-3-26. Figure 6.3-25 shows response at room temperature with the load step being that of a single bit change in ladder network. Figure 6.3-26 shows response at 125°C with full load being switched.

6.3.2.5-3 Ladder Network (Figure 6.3-27)

This network is a conventional 10-bit ladder network with the bias input at ground and the bit input at +5 v or ground, depending on the condition of the ladder switches.

For V_{ref} = +5 v

$$\text{The output} = \frac{V_{ref}}{2^n}\left[\sum_{1}^{n=10} a_n 2^{n-1}\right]$$

where n = number of bits in network

a_n = 1 or 0 depending on switch condition

The additional resistor in the network provides balanced source impedances for the comparator.

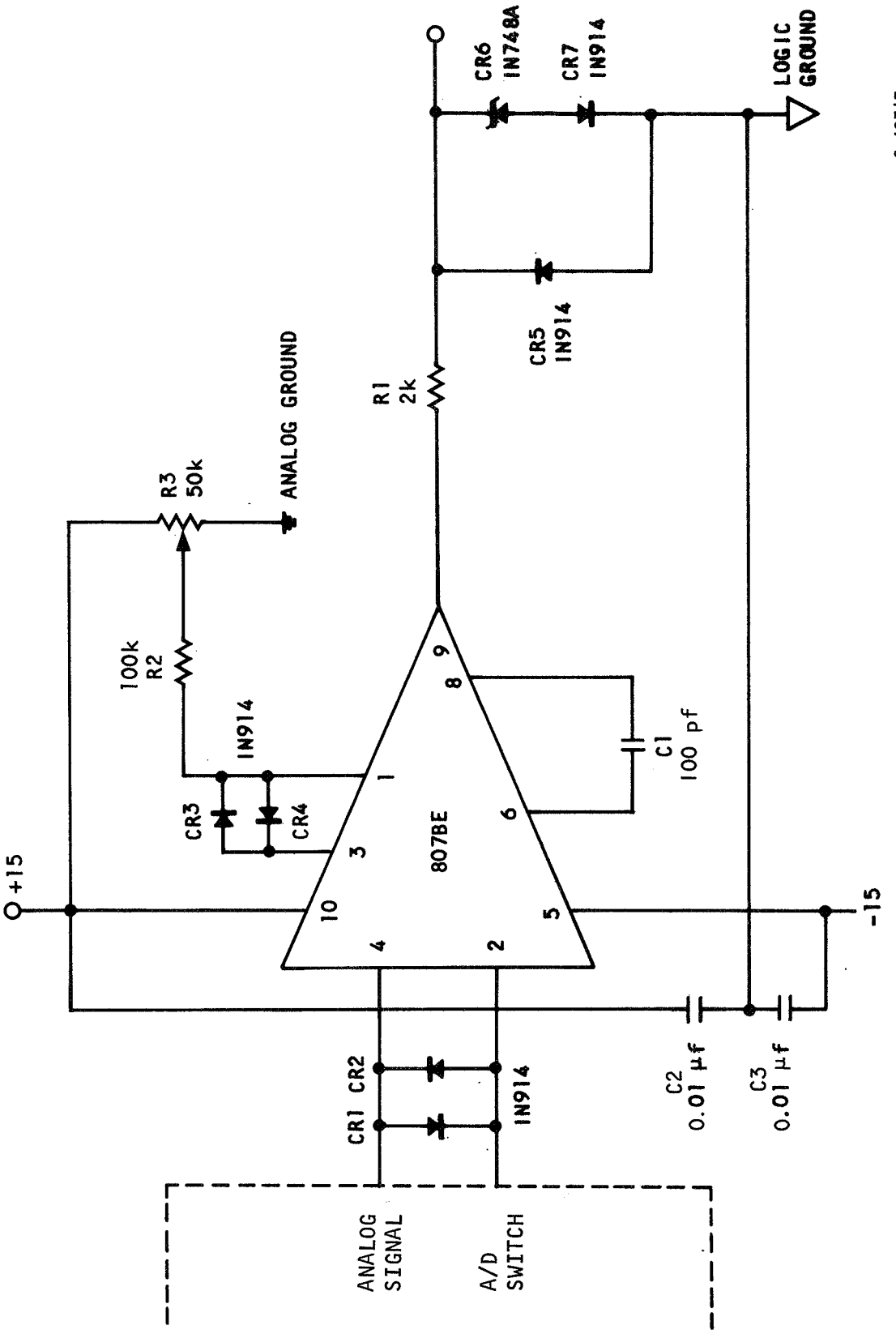


Figure 6.3-21. HRE Comparator - Thin Film (or Thick Film)

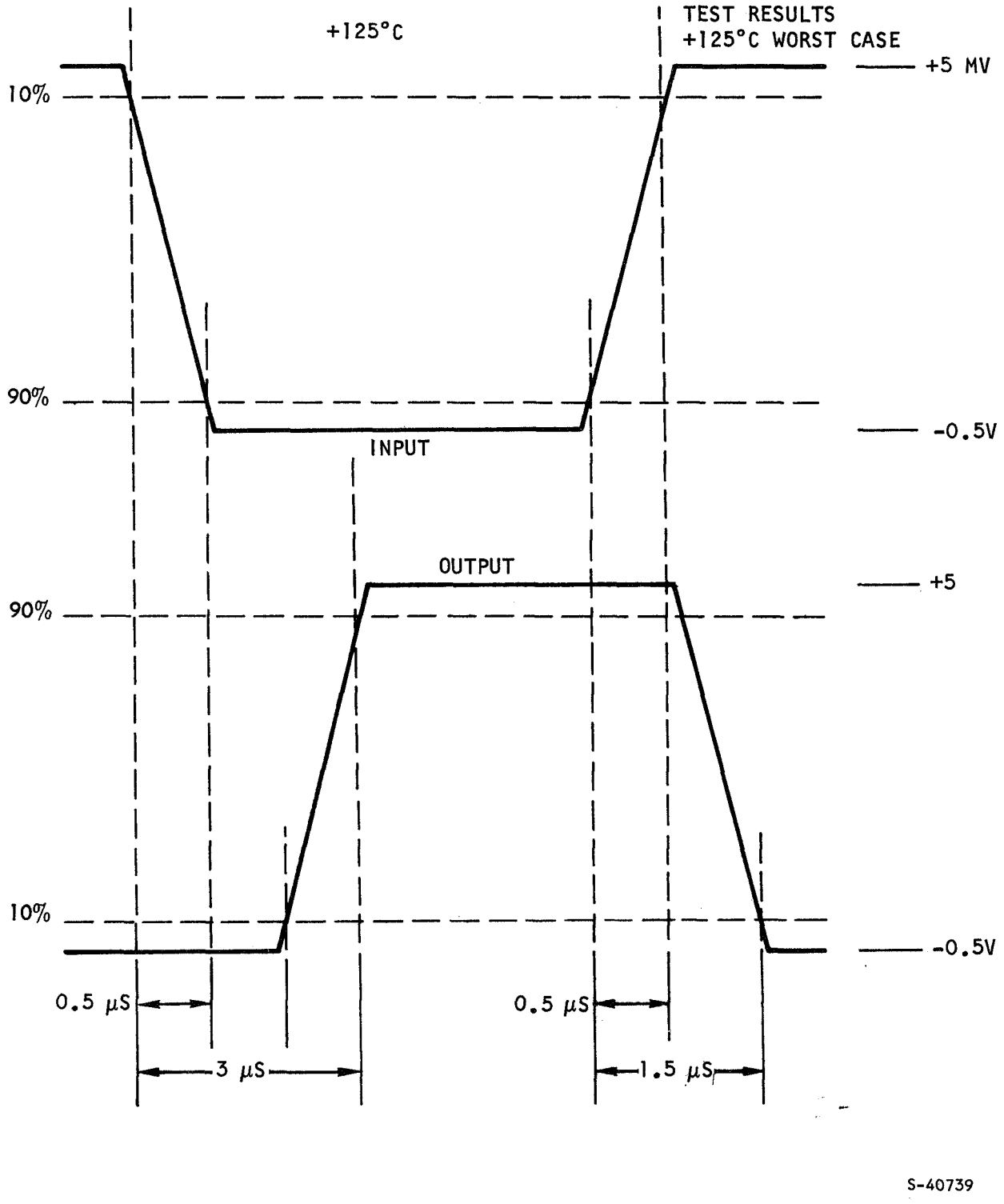


Figure 6.3-22. HRE Comparator

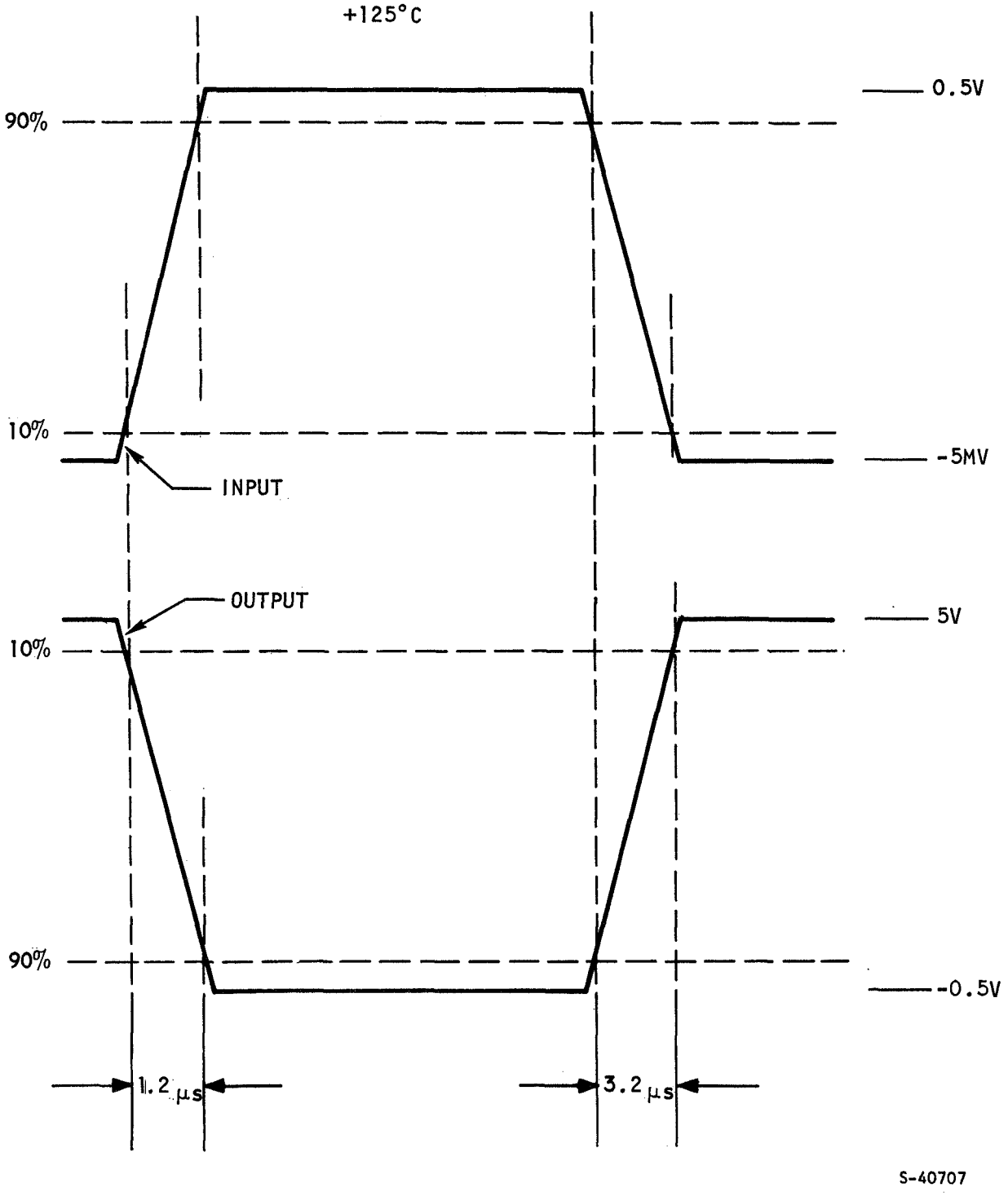


Figure 6.3-23. HRE Comparator

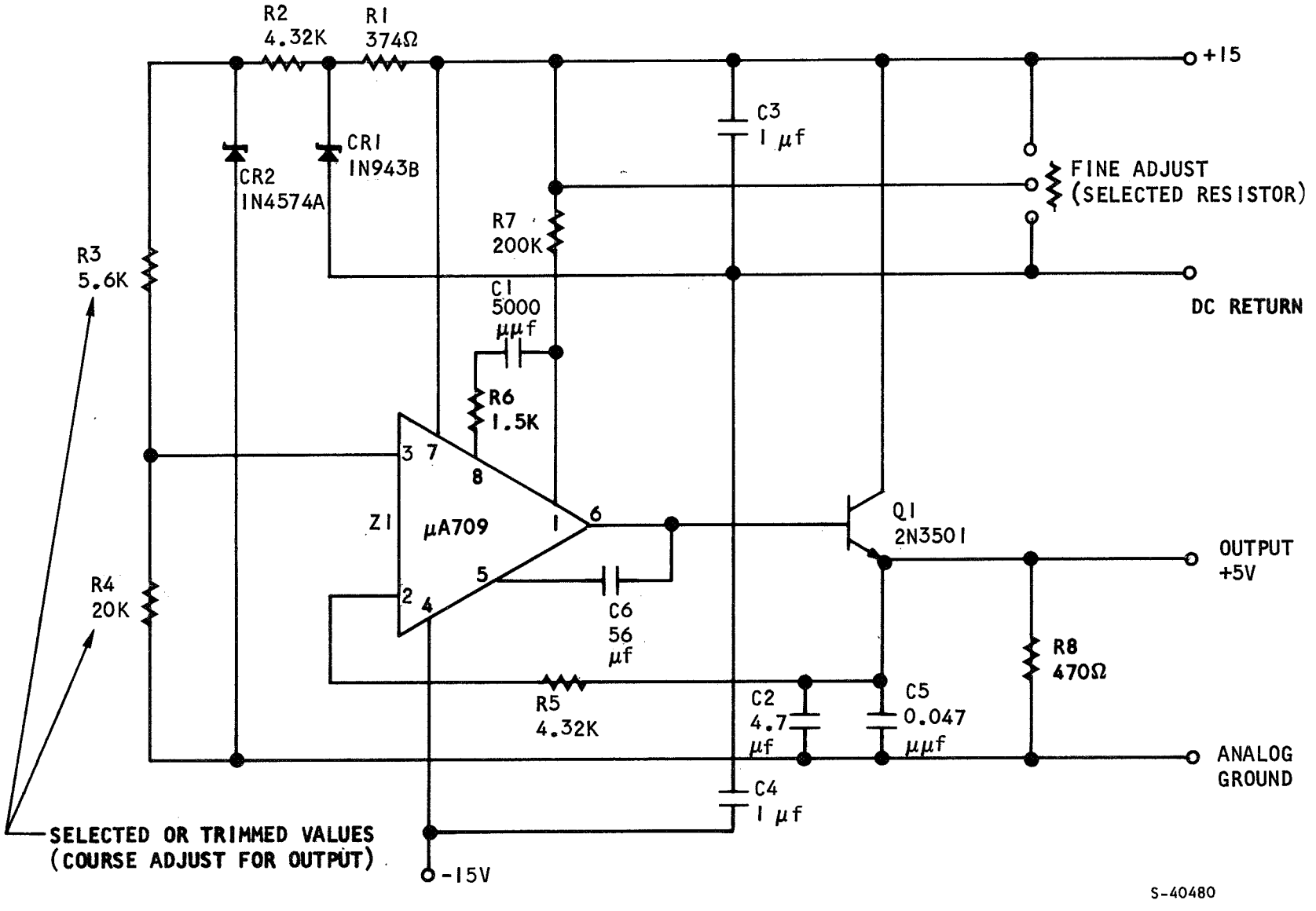


Figure 6.3-24. Ladder Reference Supply

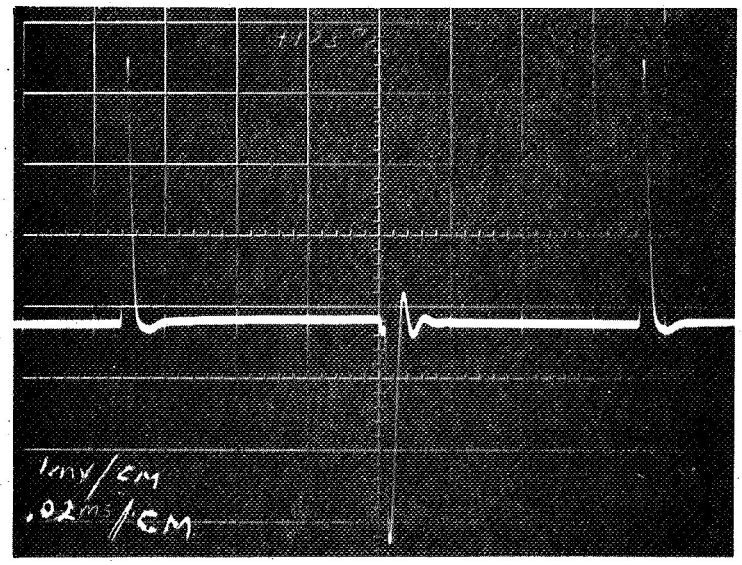


Figure 6.3-25. 5 Volt Ladder Reference Supply Response to Full Load Switching at 125°C.

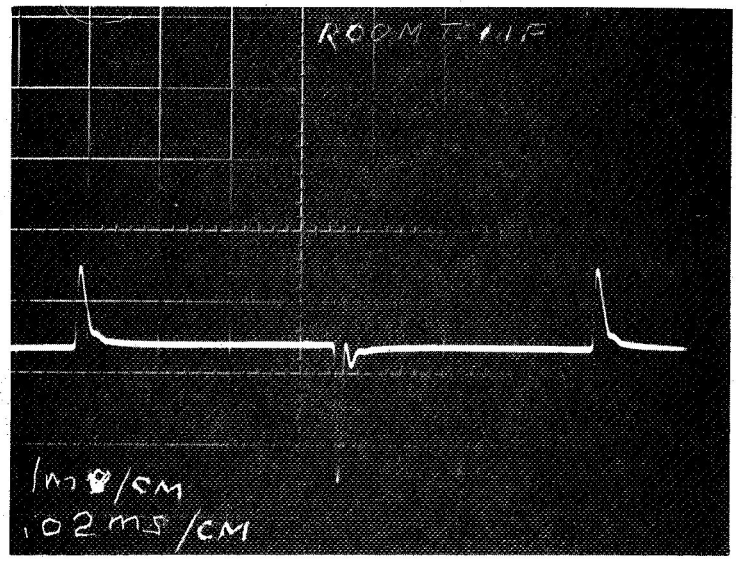


Figure 6.3-26. Response at Room Temperature with Load Step of a Single Bit in Ladder Network

F-9400

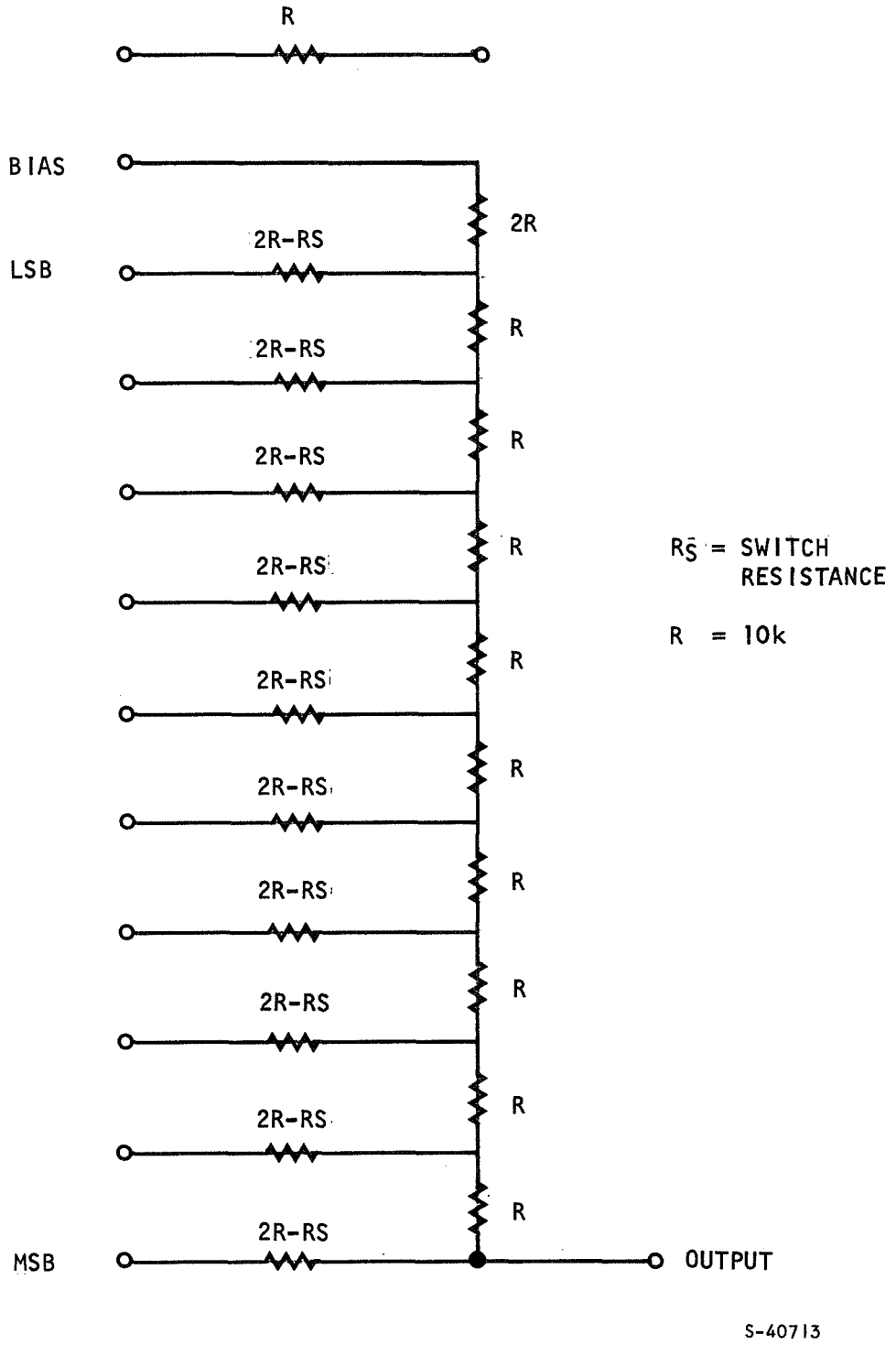


Figure 6.3-27. 10-Bit Ladder Network

6.3.2.5-4 Ladder Switch (Figure 6.3-28)

There are three single-pole double-throw switches per package. Q_2 and Q_3 are chopper transistors. When Q_1 turns off, Q_2 switches the V_{ref} line to the output; with Q_1 turned on Q_3 switches ground to the output.

Typical switching times are on the order of 0.5 μsec.

CR_1 is a Zener diode used to keep Q_2 turned off when Q_1 and Q_3 are on. CR_1 will provide a discharge path for the accumulated charge across Q_2 base to emitter when Q_2 has to be turned off. When Q_1 is turned off CR_1 will operate in the Zener region, dropping 4.7 v across it, driving current base to collector of Q_2 and causing a very low V_{ec} sat across Q_2 or $4V_{ref}$ to pin 13.

Normal input to the circuit is 0 to approximately +2.5 v and maximum input range is -0.8 v to +4 v.

Since 2N5199 has a maximum pinchoff of 4 v, the maximum common mode signal which can be presented to the LM101 is +8 v.

6.4 TEMPERATURE CONTROL

During this reporting period, circuit development effort has been directed toward completion of the individual flow channel electronics. The circuits that have been breadboarded include the multiplexer, offset and compensation, thermocouple amplifier, storage, sample and hold, and the timing circuits. This circuitry is represented in Figure 4.2-2 by the multiplexer block and the flow control block. These units have been assembled and functional testing has been initiated on the flow channel electronics exclusive of the valve driver. The valve driver for the temperature control will be essentially the same as the driver for the fuel valves shown in para. 6.3.2. Figure 6.4-1 shows the flow channel breadboard circuit group.

6.4.1 Storage Circuit

6.4.1.1 Function

This circuit senses and retains the highest of eight cyclical, conditioned thermocouple signals. At the cycle's end, switches reset the circuit output to ground potential.

The highest of eight levels continue to be produced sequentially by the storage circuit for transmission to the subsequent circuitry. This signal transmission occurs just prior to each ground reset at the conclusion of cycle.

6.4.1.2 Description (Figure 6.4-2)

Of prime importance is the storage and discharge capability of C_3. A tradeoff decision is necessary between its magnitude, insulation resistance, and surge current capabilities.

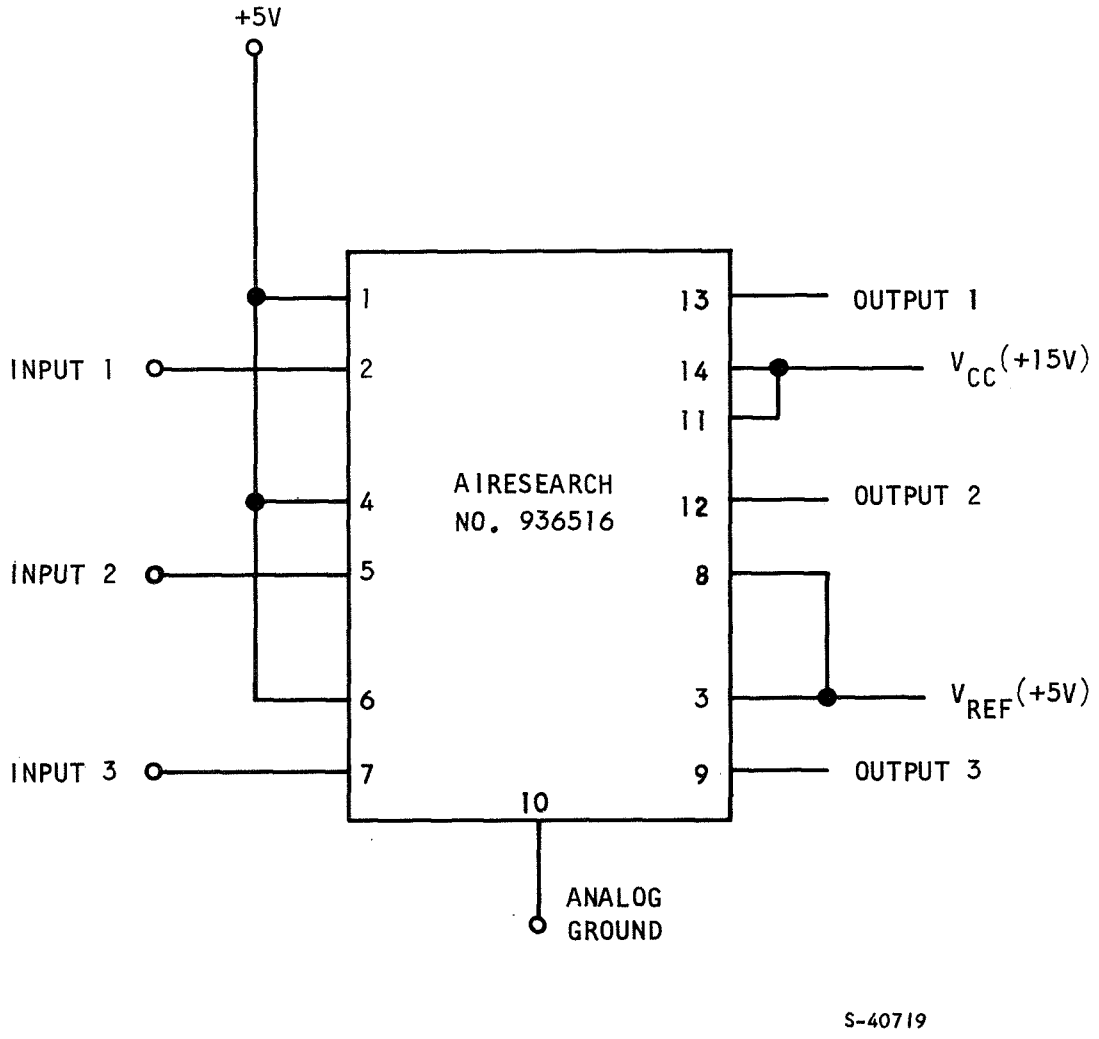
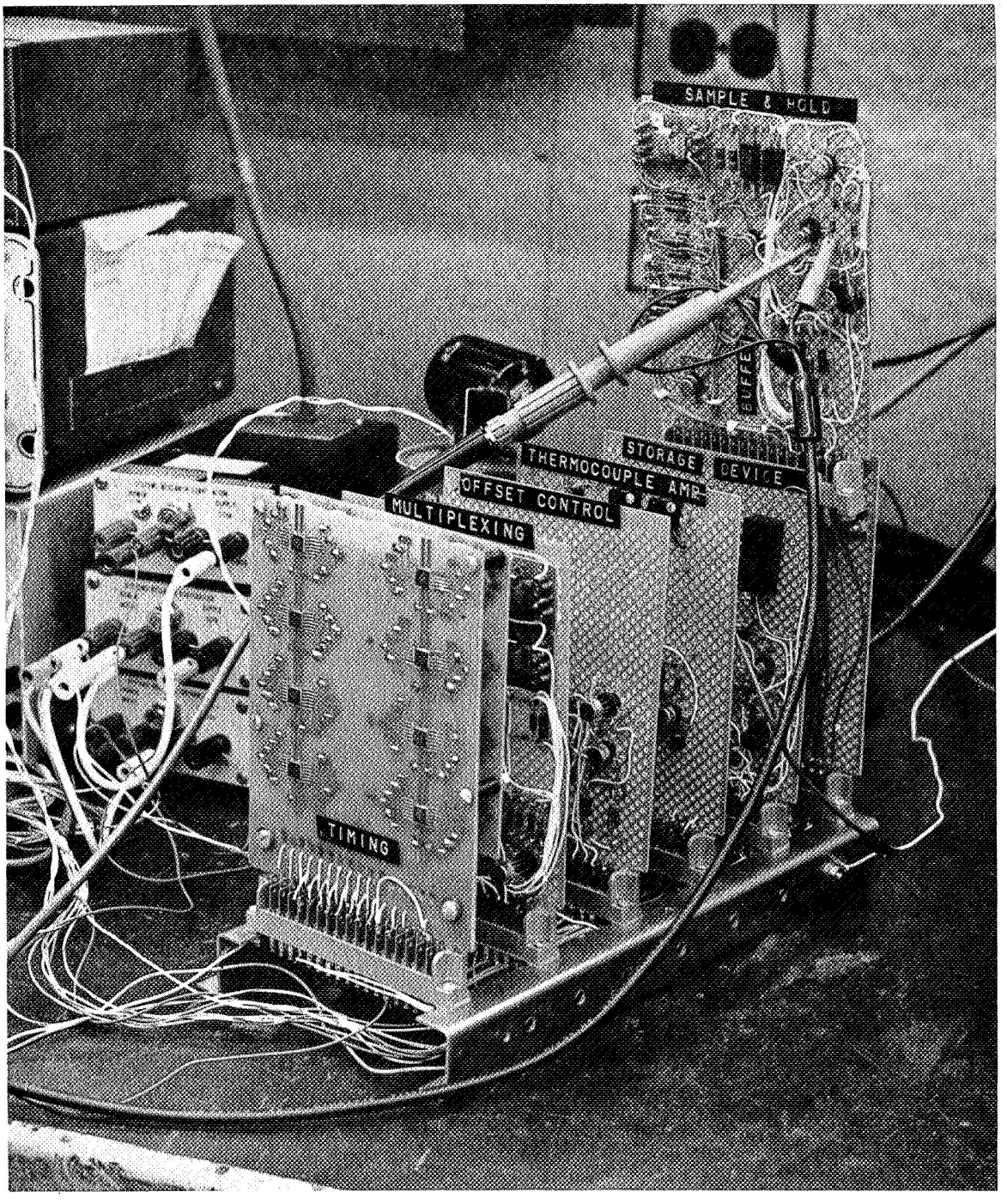


Figure 6.3-28. Ladder Switch Mechanization, 3 Bits



F-9387

Figure 6.4-1. Temperature Control Electronics Interfaced

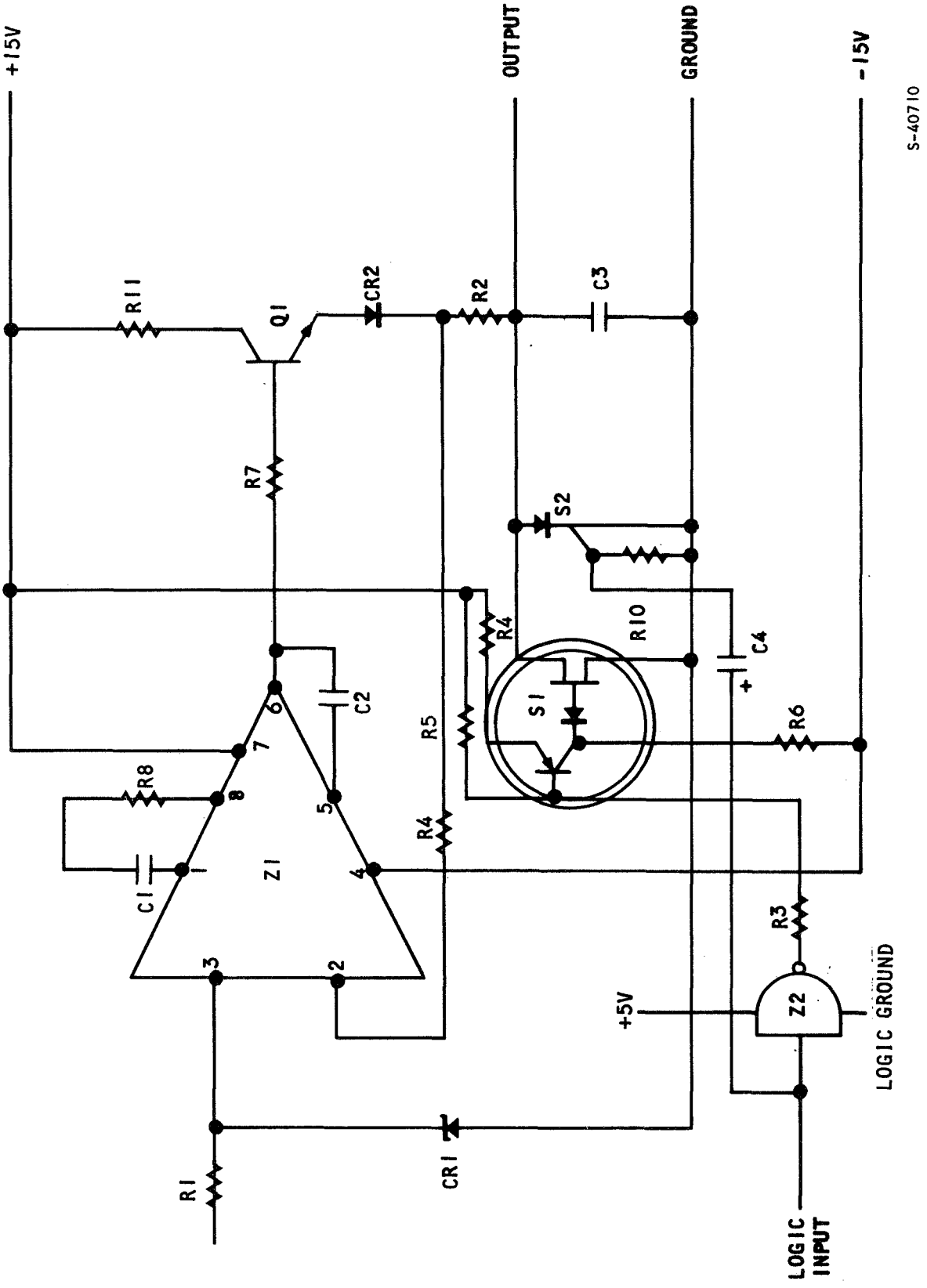


Figure 6.4-2. Storage Device Schematic

Leakage through discharge switches, and currents drawn by load and amplifier biasing must all be considered over environment in the tradeoff to ensure minimum variation in signal amplitude from the time it is sensed to the time it is transmitted.

The amplifier dynamics must be suitable to the switching application for which it is used. The capacitive load on the storage circuit inhibits feedback for a finite time period at the beginning of a cycle forcing Z_1 into saturation. Also, discharge switches, S_1 and S_2, force Z_1 into saturation when they turn on. Thus, the recovery from saturation must be fast enough not to interfere with circuit performance. In addition, during normal operation, the circuit must respond to a pulsed input quick enough yet without overshoot. The performance of the storage circuit is indicated in Figures 6.4-3 and 6.4-4.

Speed is accomplished by means of compensation components C_1, R_8, and C_2, while R_2 serves spike suppression.

Z_1 has loading limitations so Q_1 serves as a buffer stage. CR_2 protects the base-emitter junction of Q_1 against reverse biasing breakdown.

SCR (S_2) makes possible quick discharge by handling a large surge current from C_3. The need to control at low voltage levels makes it necessary to use FET switch S_1 to cancel out the offset of the SCR after initial discharge.

CR_1 protects the input stage of Z_1 from any possible spikes which exceed the circuit input ratings.

6.4.1.3 Storage Device Parts List

Z_1 - μA709 operational amplifier

Z_2 - SH2001 current driver

S_1 - 2110 BE analog gate

S_2 - IN877 SCR

Q_1 - 2N2222

CR_1 - LM103 Zener effect device

CR_2 - IN457

R_1 - 100 rs, 5%, 1/4 w, carbon composition

R_2 - 51 rs, 5%, 1/4 w, carbon composition

R_3 - 4.7 K, 5%, 1/4 w, carbon composition

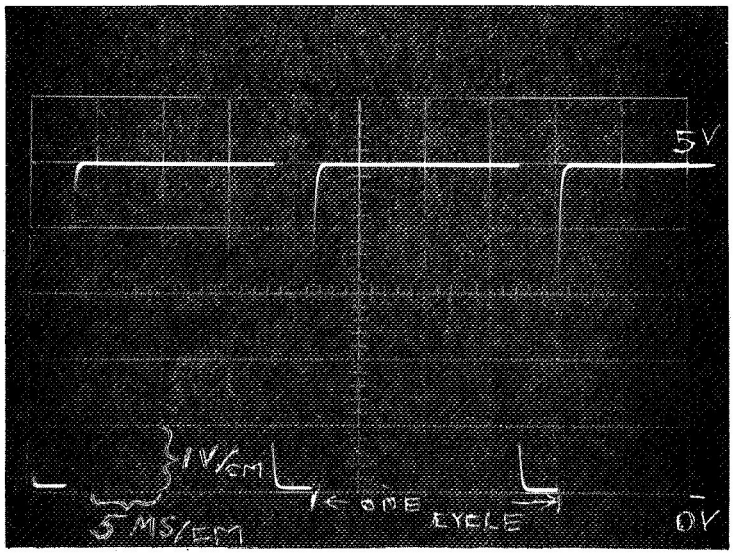
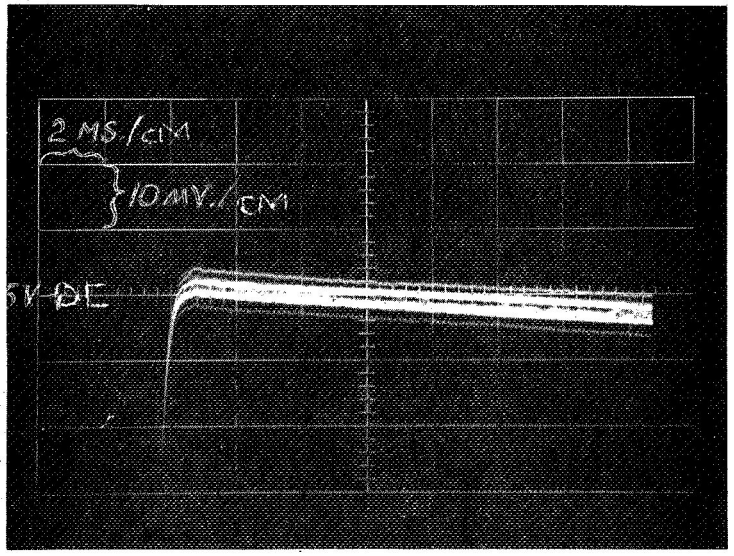


Figure 6.4-3. Performance of Storage Device as it is Driven by Multiplexing and Thermocouple Amplifier

A 2 ms duration, ±5 vdc pulse is imputed at the beginning of a cycle, followed by seven, 2 ms ground level pulses. After these, a 3 ms reset pulse brings the output to ground level, ending each cycle. Thus, the picture shows the storage device capturing the initial pulse and retaining it until reset.



F-9399

Figure 6.4-4. Storage Device Drop

With an initial 2 ms duration input at the beginning of the cycle, the storage device shows about a 5 mv signal loss in 14 ms of signal storage.

R_4 - 220 r, 5%, 1/4 w, carbon composition

R_5 - 510 rs, 5%, 1/4 w, carbon composition

R_6 - 10 K, 5%, 1/4 w, carbon composition

R_7 - 300 r, 5%, 1/4 w, carbon composition

R_8 - 1.5 K, 5%, 1/4 w, carbon composition

R_9 - 100 rs, 5%, 1/4 w, carbon composition

R_{10} - 1 K, 5%, 1/4 w, carbon composition

R_{11} - 100 r, 5%, 1/4 w, carbon composition

C_1 - 100 pf, 10%, 35 wvdc, NP

C_2 - 5 pf, 10%, 35 wvdc, NP

C_3 - 3 uf, 5%, 20 wvdc, NP

C_4 - 0.1 uf, 10%, 35 wvdc, polar

6.4.2 Buffer Stage

6.4.2.1 Function

Isolation between the capacitive output storage circuit and capacitive input sample and hold circuit is accomplished by adding an interstage with very low output impedance. The current sinking and delivery capabilities needed to drive a capacitive load are achieved in this stage.

6.4.2.2 Description

The amplifier is in a voltage-follower configuration. Z_1 provides the high open-loop gain necessary to attain the near infinite input impedance and zero output impedance.

The emitter-coupled/base-coupled transistors, Q_1 and Q_2, allow both output current delivery and current drain to drive the capacitive load.

CR_1 and CR_2 protect the input stage of Z_1 from exceeding common mode input rating.

Performance of the buffer stage is indicated in Figures 6.4-5, 6.4-6, and 6.4-7.

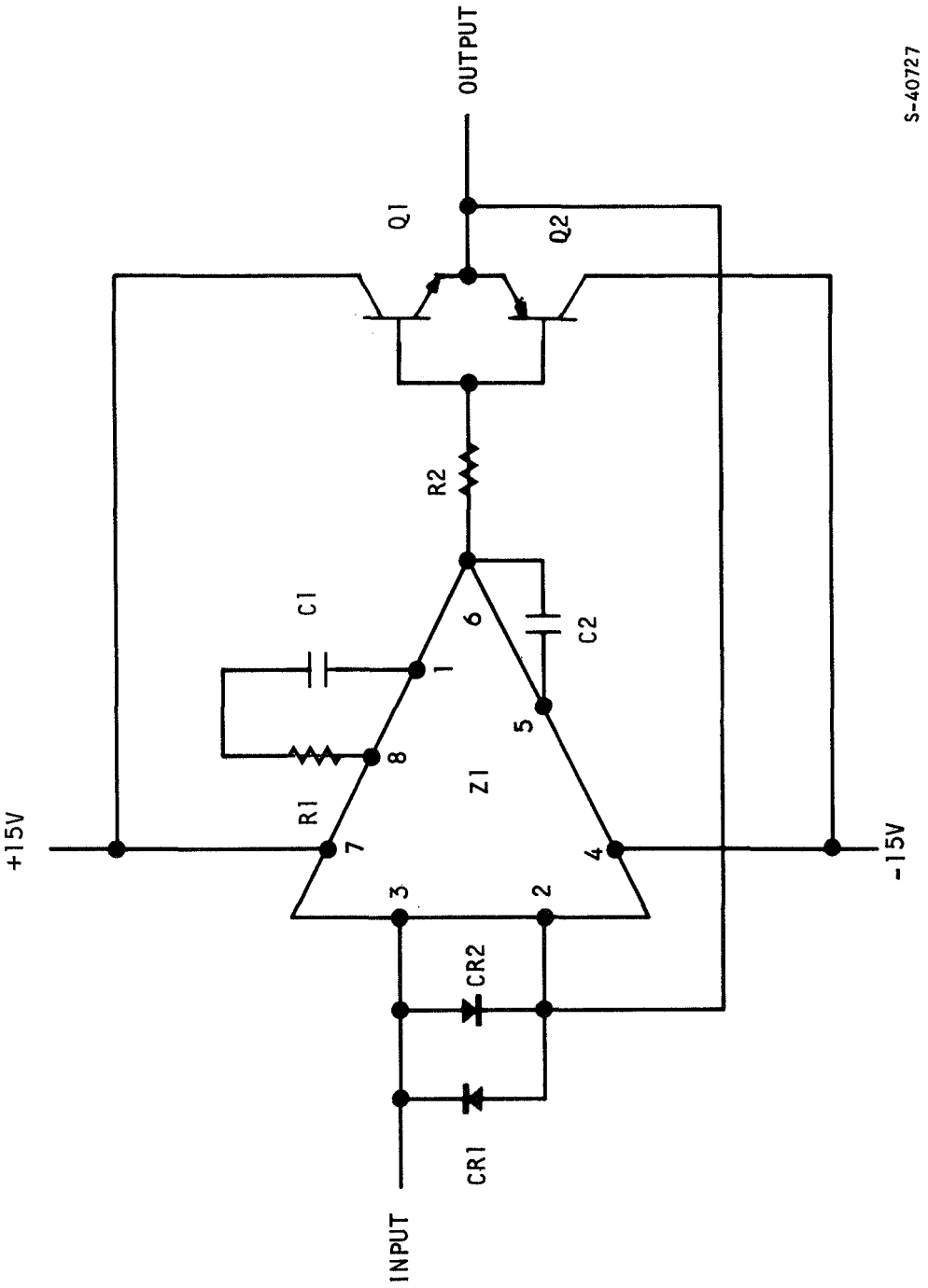


Figure 6.4-5. Buffer Amplifier Schematic

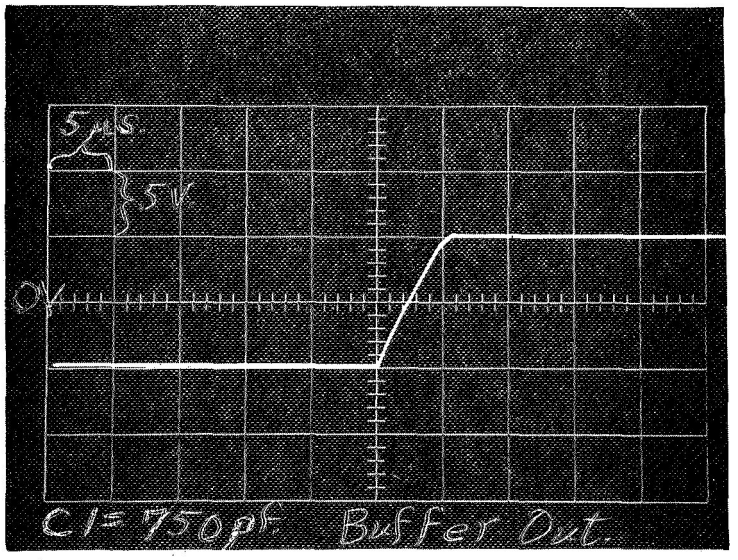
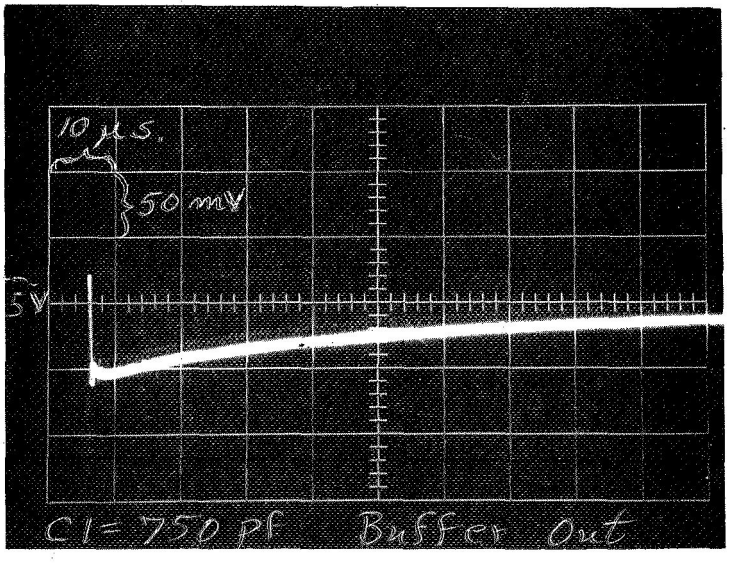


Figure 6.4-6. Response of Buffer Amplifier to Step Input



F-9397

Figure 6.4-7. High Gain View of Buffer Amplifier Overshoot and Recovery Time in Response to Step Input

6.4.2.3 Buffer Amplifier Parts List

Z_1 - uA709

Q_1 - 2N2222

Q_2 - 2N2907

CR_1 - IN457

CR_2 - IN457

R_1 - 1.5 K, 1/4 w, 5%, carbon composition

R_2 - 500 rs, 1/4 w, 5%, carbon composition

C_1 - 200 pf, ±10%, 40 wvdc, nonpolar

C_2 - 20 pf, ±10%, 40 wvdc, nonpolar

6.4.3 Sample and Hold

6.4.3.1 Function

It is necessary to sample the resulting signal from the peak detector (storage circuit) and hold it over a time period during which it is used as a control signal. This signal must be accurately updated after each successive cycle conclusion. The sample and hold circuit serves this purpose.

6.4.3.2 Description

FET switch S_2 closes to allow signal transmission to the amplifier. S_2 then opens leaving C_1 to store the signal level until S_2 closed again. S_1 closes simultaneously with S_2, making Z_1 a voltage-follower amplifier.

When S_1 opens, C_3 begins to charge up. This feedback effect around Z_1 compensates for the droop of C_1 and thus tends to keep the output constant until a new signal level is transmitted. This allows the use of relatively low capacitance values for C_1 and C_3. The effectiveness of this compensation depends on the matching of leakages through C_1 and C_3.

The performance of the sample and hold circuit is indicated in Figures 6.4-8, 6.4-9, 6.4-10, and 6.4-11.

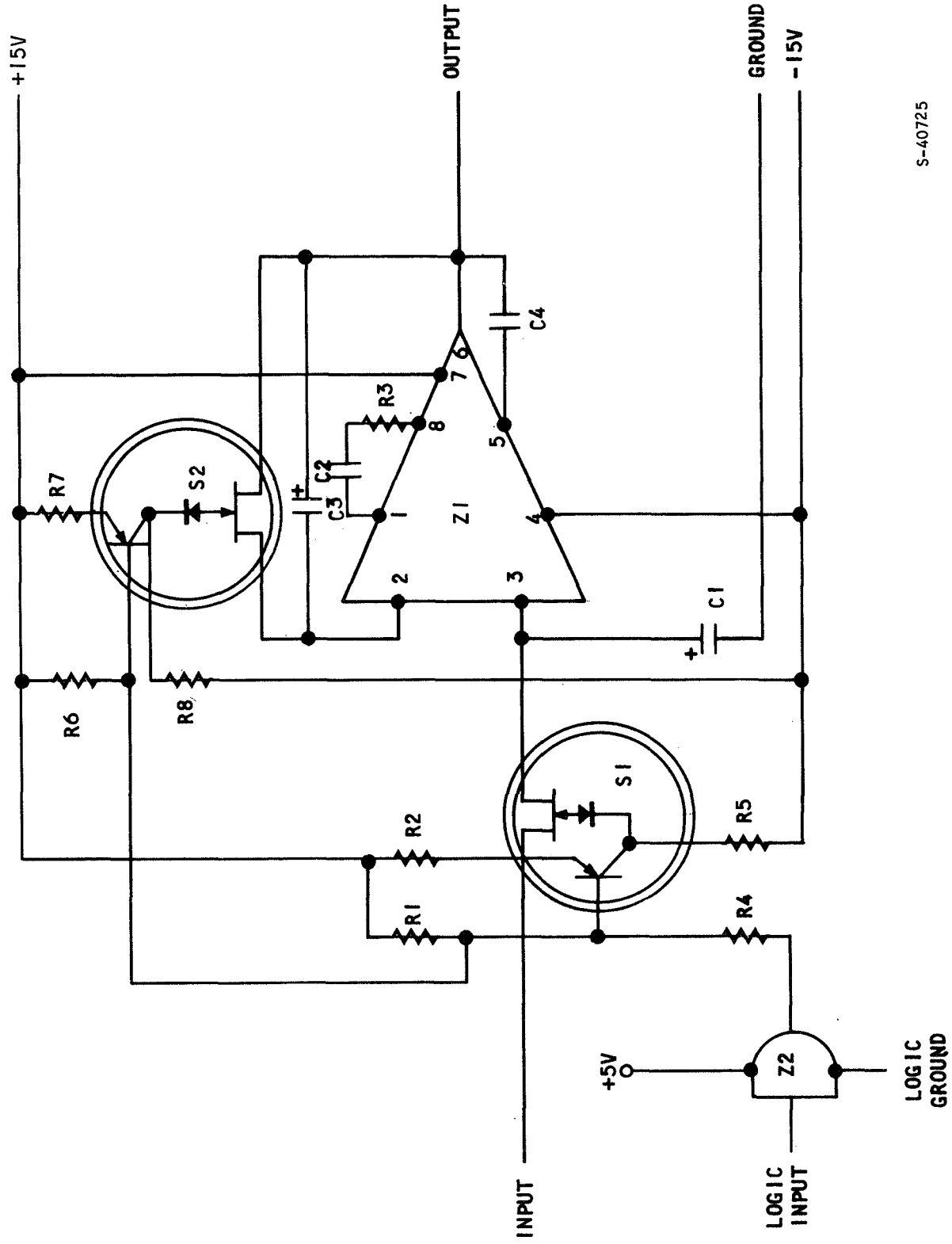


Figure 6.4-8. Sample and Hold Circuit Schematic

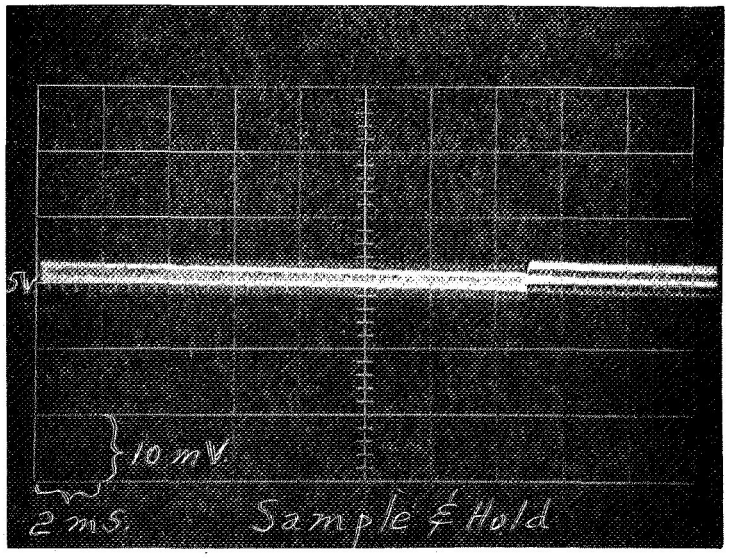
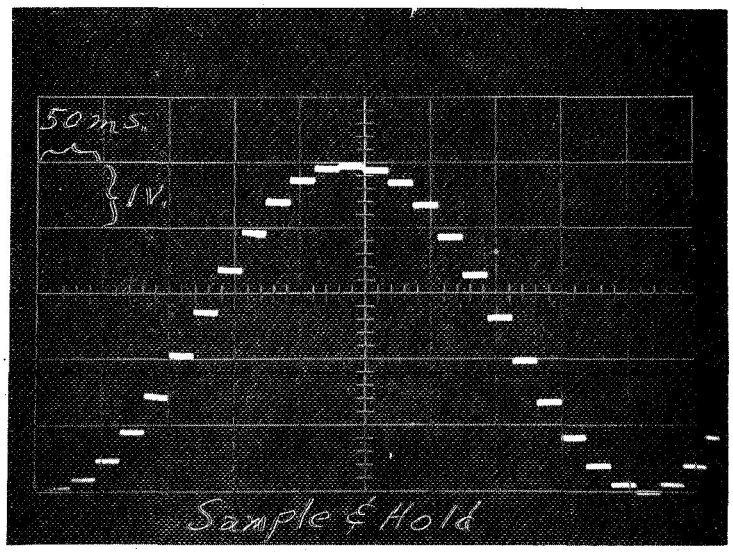


Figure 6.4-9. Sample and Hold Circuit Signal Loss Over One Cycle

The abrupt voltage level change denotes the conclusion of one cycle and the updating of signal to its original value. An approximate 5 mv signal loss is shown over one cycle.



F-9401

Figure 6.4-10. Sine Wave Reconstruction

A 1 cps sine wave is multiplexed into the thermocouple amplifier and the storage circuit creates periodic level signals for transmission to Sample and Hold. The picture shows this circuit capturing the signal, retaining it, and being updated at the conclusion of each multiplexing cycle.

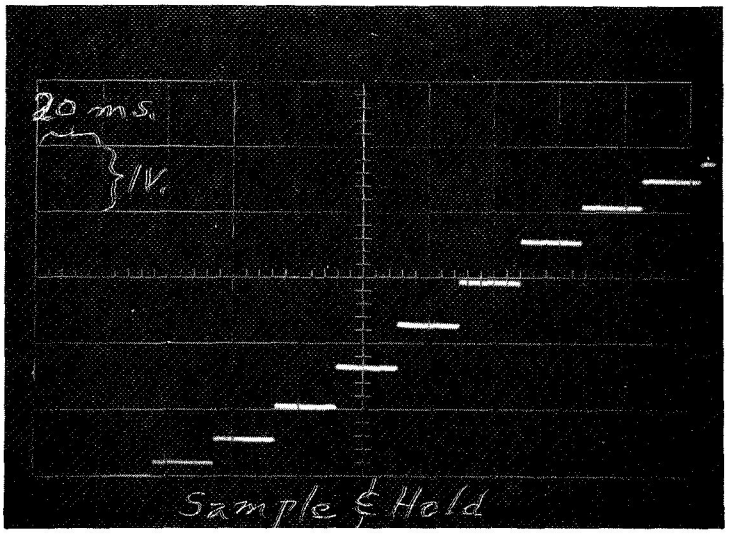


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Figure 6.4-11. Time Scale Expansion of Figure 6.4-7

6.4.3.3 Sample and Hold Circuit Parts List

Z_1 - uA709 operational amplifier

Z_2 - SH2001 current driver

S_1 - 2110 BE analog gate

S_2 - 2110 BE analog gate

R_1 - 510 ohm, 5%, 1/4 w, carbon composition

R_2 - 220 ohm, 5%, 1/4 w, carbon composition

R_3 - 1.5 K, 5%, 1/4 w, carbon composition

R_4 - 2.4 K, 5%, 1/4 w, carbon composition

R_5 - 10 K, 5%, 1/4 w, carbon composition

R_6 - 510 ohm, 5%, 1/4 w, carbon composition

R_7 - 220 ohm, 5%, 1/4 w, carbon composition

R_8 - 10 K, 5%, 1/4 w, carbon composition

C_1 - 1 uf, 5%, 35 wvdc, polar

C_2 - 1500 pf, ±10%, 35 wvdc, NP

C_3 - 1 uf, 5%, 3.5 wvdc, polar

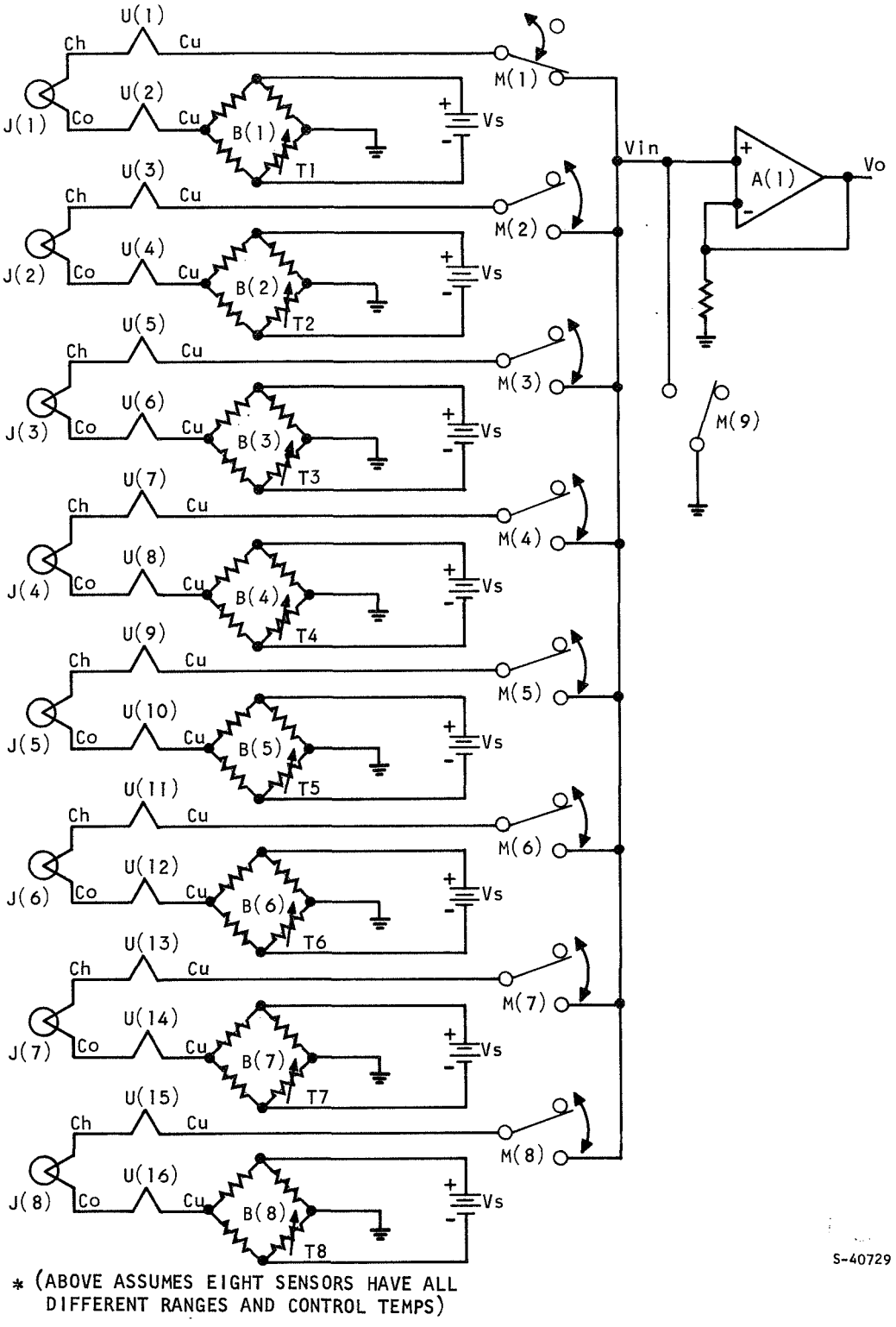
C_4 - 200 pf, ±5%, 35 wvdc, NP

6.4.4 Input Offset and Compensation Mechanization

6.4.4.1 Description

Two methods of temperature compensating the thermocouple junctions and offsetting their outputs have been considered. The first method involves incorporating the compensation and offsetting into a resistive bridge for each thermocouple with a different control temperature (Figure 6.4-12). The second uses one bridge with zero offset for all thermocouples and depends on sequentially switching in the offsets (Figure 6.4-13).

The first method has the advantage of allowing variation of each bridge to suit each individual sensor and thus improve attainable accuracy. This method also avoids electronics problems associated switching signals into amplifiers. The size and cost of this technique, as compared to the alternative, make the alternative more desirable.



* (ABOVE ASSUMES EIGHT SENSORS HAVE ALL DIFFERENT RANGES AND CONTROL TEMPS)

Figure 6.4-12. Compensation Configuration, Alternate I

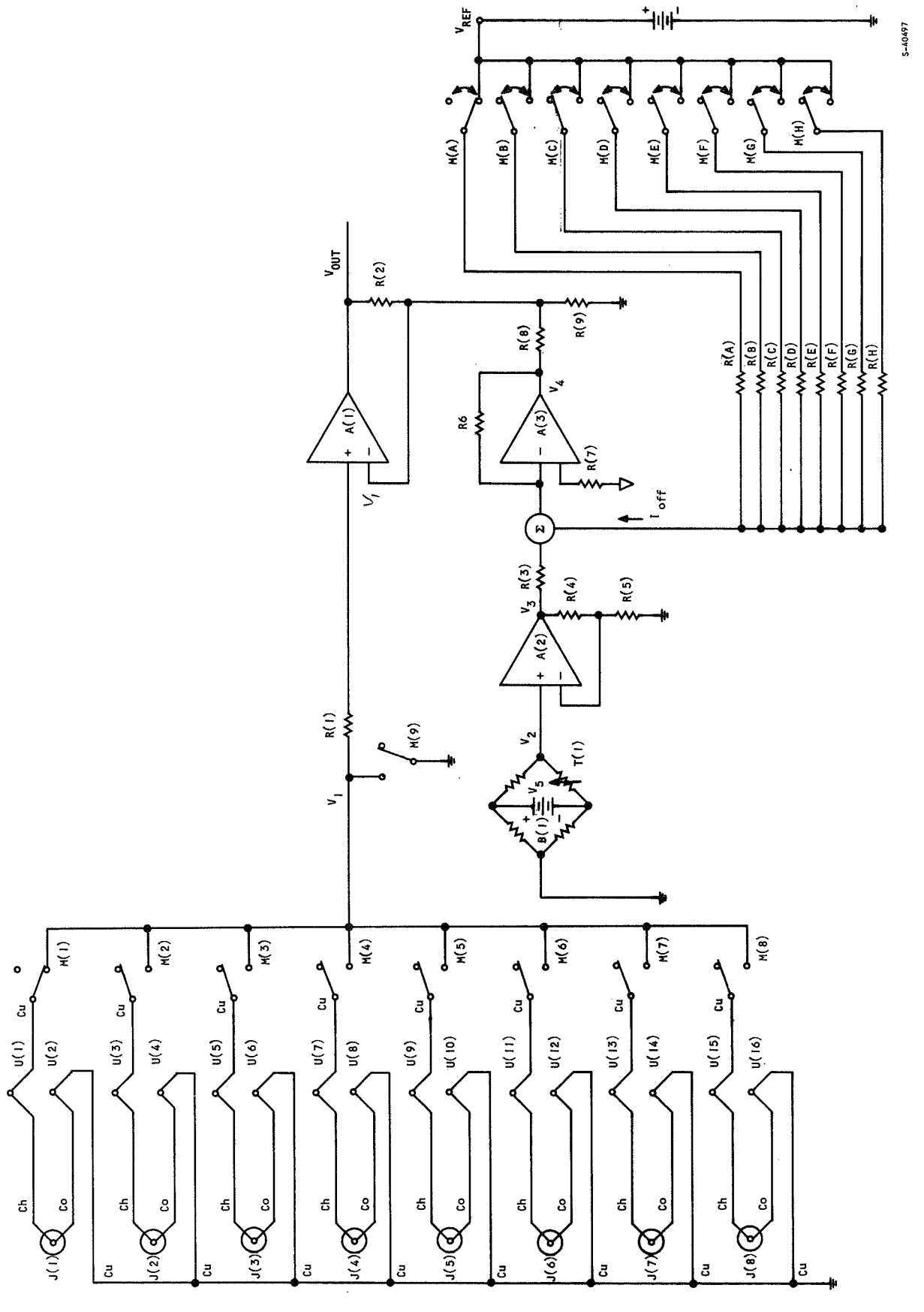


Figure 6.4-13. Compensation Configuration, Alternate 2

The accuracy of this second method depends on the repeatability of thermocouple characteristics, since one thermometer is used to compensate all sensors. One advantage is that the offsets are introduced after the thermocouple signals have been conditioned by the thermocouple amplifier. Noise and environment sensitivity of offsets are thus reduced. This method also reduces appreciably the power requirement from that needed when separate bridges are used.

Comparisons of cost and size have influenced the decision to attempt this second mechanization.

6.4.4.2 Symbol Definitions for Figures 6.4-12 and 6.4-13

(1) J(X) - Thermocouple hot junction (sensor)

(2) U(X) - Thermocouple cold junction

(3) T(X) - Thermometer resistor

(4) B(X) - Compensator bridge

(5) M(X) - Solid-state multiplex switch

(6) A(X) - Amplifier

(7) Cu - Copper Metal

(8) Co - Constantan metal

(9) Ch - Chromel metal

6.4.4.3 Explanation of Figure 6.4.4.2

It is assumed that a different offset is required for each sensor. Thus, one sensor multiplex switch (M1→M8) closes simultaneously with each appropriate offset multiplex switch (MA→MH) and R(A)→R(B) determine the amount of offset.

The compensator bridge is in the same environment as the cold junction. It is calibrated to yield the same gain and same voltage magnitude as the combination of cold junctions associated with any one sensor.

A(2) conditions the compensator output (V_g), and A(3) sums this signal (V_3) with the offset signal. The resultant is then introduced into the thermocouple amplifier, A(1), along with the thermocouple signal (V_1). V_{out} is derived as follows: (Figure 6.4-13)

(1) $$\frac{V_{out} - V_1}{R_2} + \frac{V_4 - V_1}{R_8} = \frac{V_1}{R_9}$$

(2) $$\frac{V_{out}}{R_2} = \frac{V_1}{R_9} - \frac{(V_4 - V_1)}{R_8} + \frac{V_1}{R_2}$$

(3) $$V_{out} = R2V_1 \left(\frac{1}{R_9} + \frac{1}{R_8} + \frac{1}{R_2}\right) - \frac{V_4}{R_8} R_2$$

(4) $$V_{out} = V_1 \left[\frac{R2^2(R8 + R9) + R8 \cdot R9 \cdot R2}{R8 \cdot R9 \cdot R2}\right] - V_4 \frac{R2}{R_8}$$

$$= V_1 \frac{R2 \cdot R8 + R2 \cdot R9 + R8 \cdot R9}{R8 \cdot R9} - V_4 \frac{R2}{R_8}$$

(5) $$V_4 = V_2 \frac{(R_4 + R_5)}{R5} \frac{R6}{R3} + V_{ref} \frac{R6}{R(X)}$$

where R(X) = appropriate switched in value)

(6) $$\text{So } V_{out} = V_1 \left[\frac{R2 \cdot R8 + R2 \cdot R9 + R8 \cdot R9}{R8 \cdot R9}\right]$$

$$- V_2 \left[\frac{R2(R4 + R5)R6}{R_8 R5 R3}\right] - V_{ref} \left[\frac{R2 \cdot R6}{R_8 \cdot R(X)}\right]$$

6.4.5 Clock

6.4.5.1 Requirements

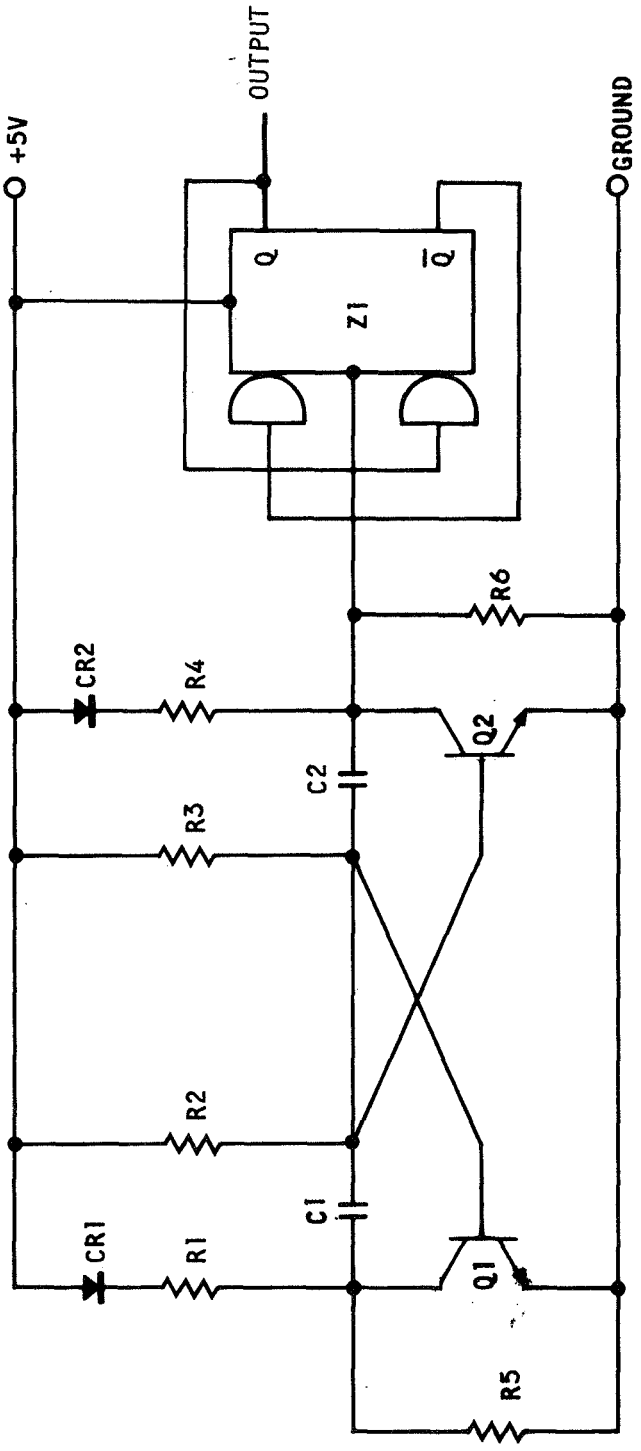
A free-running clock is necessary to provide the basic frequency for the digital timing control. An astable multivibrator is sufficient for this purpose, since the fixed-frequency accuracy is only critical to within ±10 percent because of the response limitations of the electronics.

The fixed duty cycle, likewise, can vary over a wide range without adversely affecting performance, since a logic network divides the basic frequency by 2 and switches only on the falling edge of each clock pulse. This logic network also acts as a buffer stage which squares up the clock pulse waveform and isolates from the clock the loading by digital timing control circuitry.

The relatively low frequency desired (500 cps) also favors such a simple circuit.

6.4.5.2 Description (Figure 6.4-14)

Calculations and breadboard testing prove the fact that the collect-coupled, astable multivibrator supplies a 500-cps ±10 percent pluse train with duty cycle variation of less than 1 percent over environment and power supply transients.



S-40716

Figure 6.4-14. Astable Multivibrator

Q_1 and Q_2 have large base-emitter reverse voltage ratings (7 v max.) compared to most other transistors of the same size and power ratings. This enables them to take the -5 v reverse voltage applied upon switching states.

CR_1 and CR_2 compensate for the V_{BE} temperature variation of Q_1 and Q_2 and thus keep the frequency more stable over environment. R_5 and R_6 make it possible to keep CR_1 and CR_2 turned on when Q_1 and Q_2 are off.

The clock frequency is determined by the time constants R_2C_1 and R_3C_2. These components are, therefore, precision valued with low-temperature coefficients.

Z_1 is a J-K flip-flop used to square up the clock output and isolate the load.

Temperature tests on breadboards circuitry revealed variation in the frequency output of the clock of less than 3 percent.

Frequency dependence on power supply variation is logarithmic so the predictable supply charge causes a frequency change of less than 1 percent as supported by test results.

6.4.5.3 Parts List for Clock

Q_1 - 2N910

Q_2 - 2N910

CR_1 - IN457

CR_2 - IN457

Z_1 - DtuL 945

C_1 - 0.1 uf, 1 percent SOU

C_2 - 0.1 uf, 1 percent SOU

R_1 - 390 K, ±5 percent, 1/4 w

R_2 - 7.21 K, 0.25 percent, 1/8 w, 25 ppm/°C

R_3 - 7.21 K, 0.25 percent, 1/8 w, 25 ppm/°C

R_4 - 390 K, ±5 percent, 1/4 w

R_5 - 100 K, 5 percent, 1/4 w

R_6 - 100 K, 5 percent, 1/4 w

6.5 SYSTEM INTEGRATION

The rack assembly which will house the complete breadboard system is shown in Figure 6.5-1.

The top part of the assembly contains the fuel control loop, together with stimuli and display facilities; the lower part will contain the temperature control loop, also with stimuli and display facilities.

Initially, system integration will involve the use of the computer test console to take advantage of the teletype interface and computer display facilities. Later, when the fuel control loop contains a teletype interface, it will be possible tc divorce the GSE from the control systems.

At the present time the rack assembly contains only the digital portion of the interface which has been checked out functionally.

Figures 6.5-2 and 6.5-3 show the hardware associated with stimuli/display and digital interface, respectively.

The digital circuit boards can be withdrawn and hinged for checkout; the drawer, as a whole, will have the computer mounted on the rear face, and can be withdrawn for oven temperature testing.

The unused board positions of the drawer will house the analog portion of the fuel control system, together with the teletype interface for the computer.

Figure 6.5-4 shows the stimuli/display facilities associated with the fuel control loop.

The top-left section contains a display for the contents of the main I/O transfer register and a calibration check facility for the ADC.

The center-left section contains a computer output-interface simulator, which enables the system to be checked out with simulated computer instructions. The instructions are set-up by the two rows of switches and transferred into the interface by an initiate signal.

The lower-left section contains display facilities for apcode and address memories, discrete output memories, and the analog output multiplexer.

It also contains switches for simulating the discrete inputs.

The right half of the stimuli/display unit contains potentiometers for simulating analog inputs, together with a lamp display to verify correct input selection by the multiplexer.

Analog signals, both inputs and outputs, can be accurately measured using the digital voltmeter mounted above the stimuli/display panel. Signals are switched into the voltmeter using the selectors mounted at the top-right of the panel.

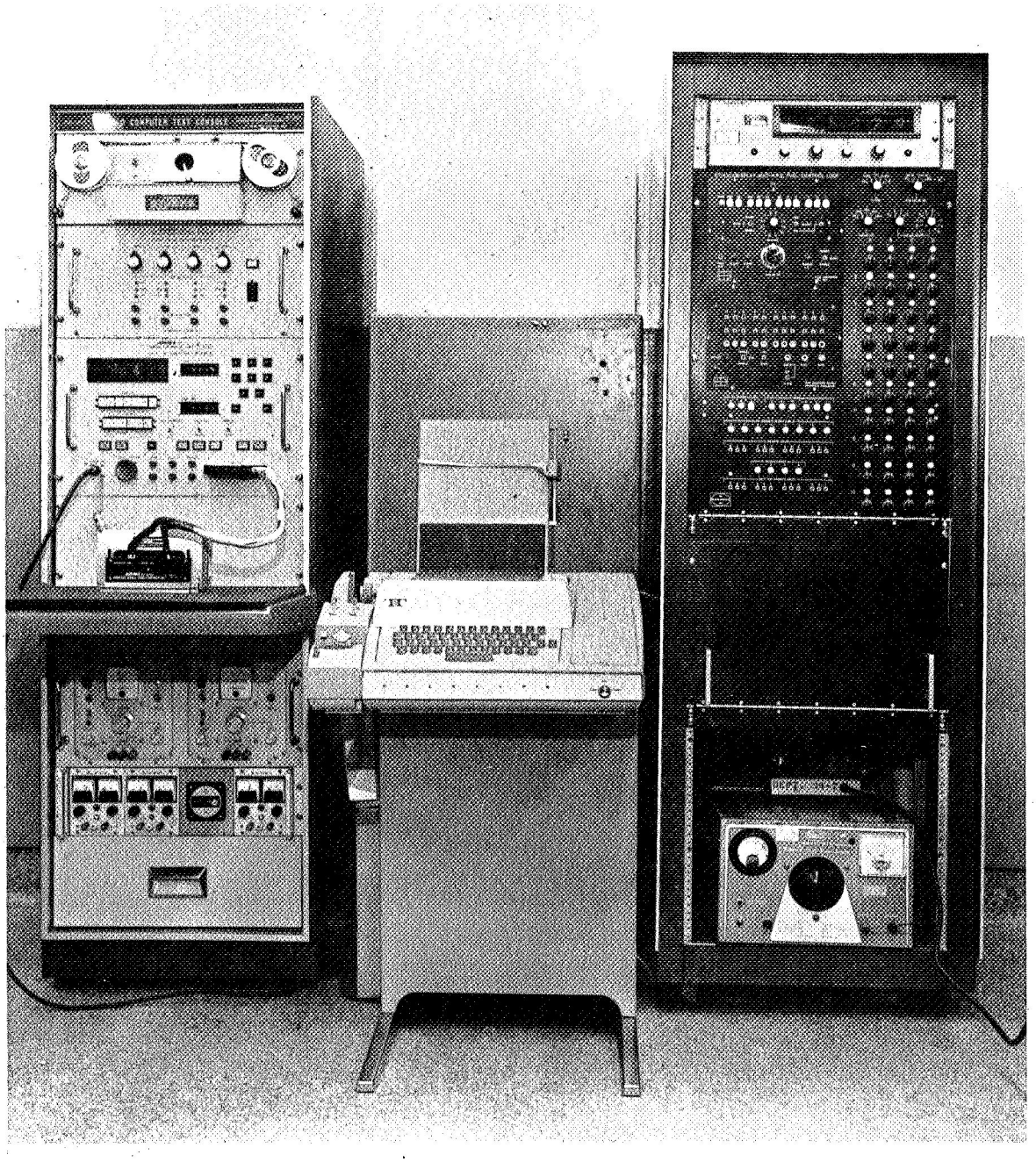


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Figure 6.5-1. Control System Rack Assembly

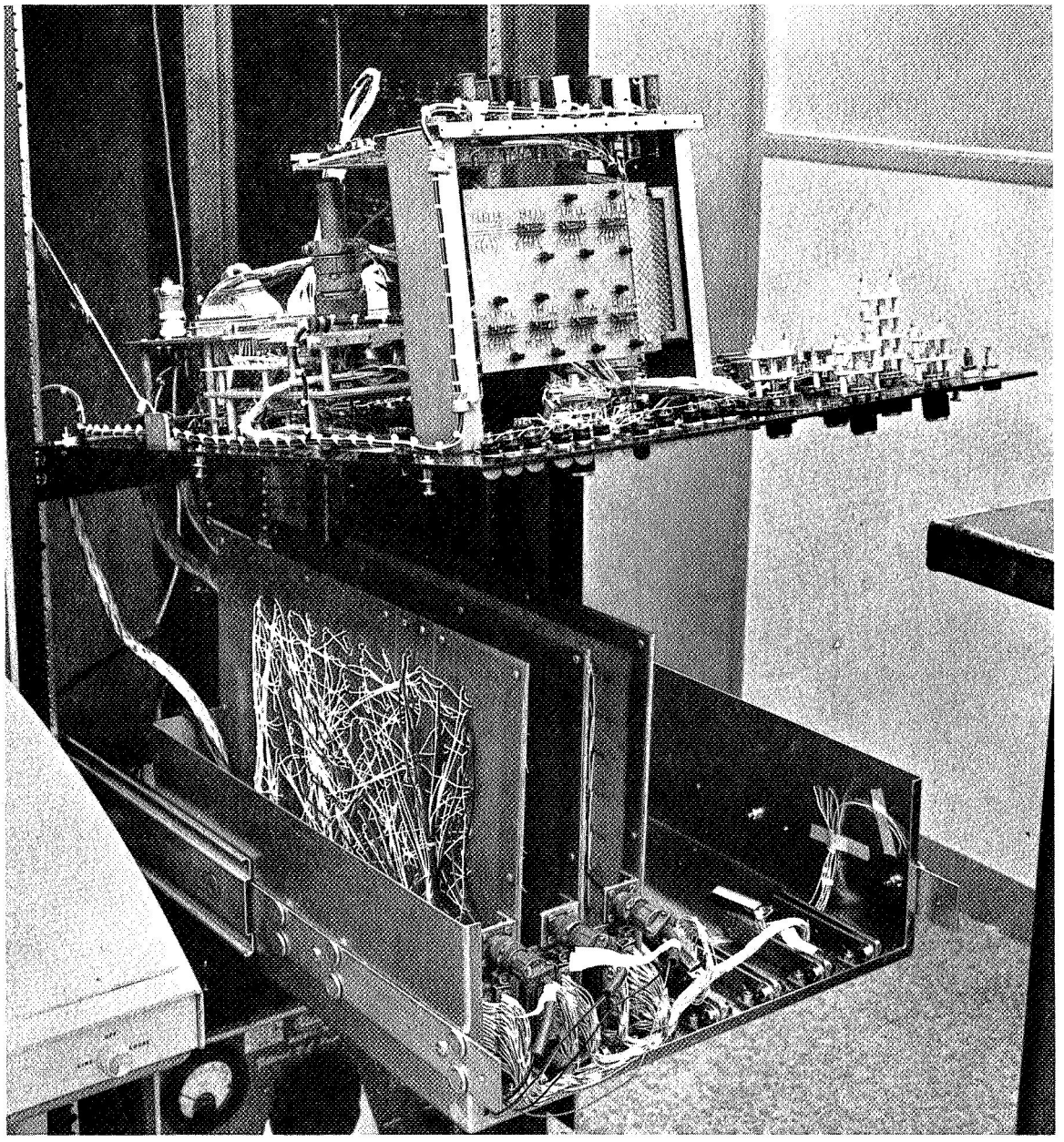
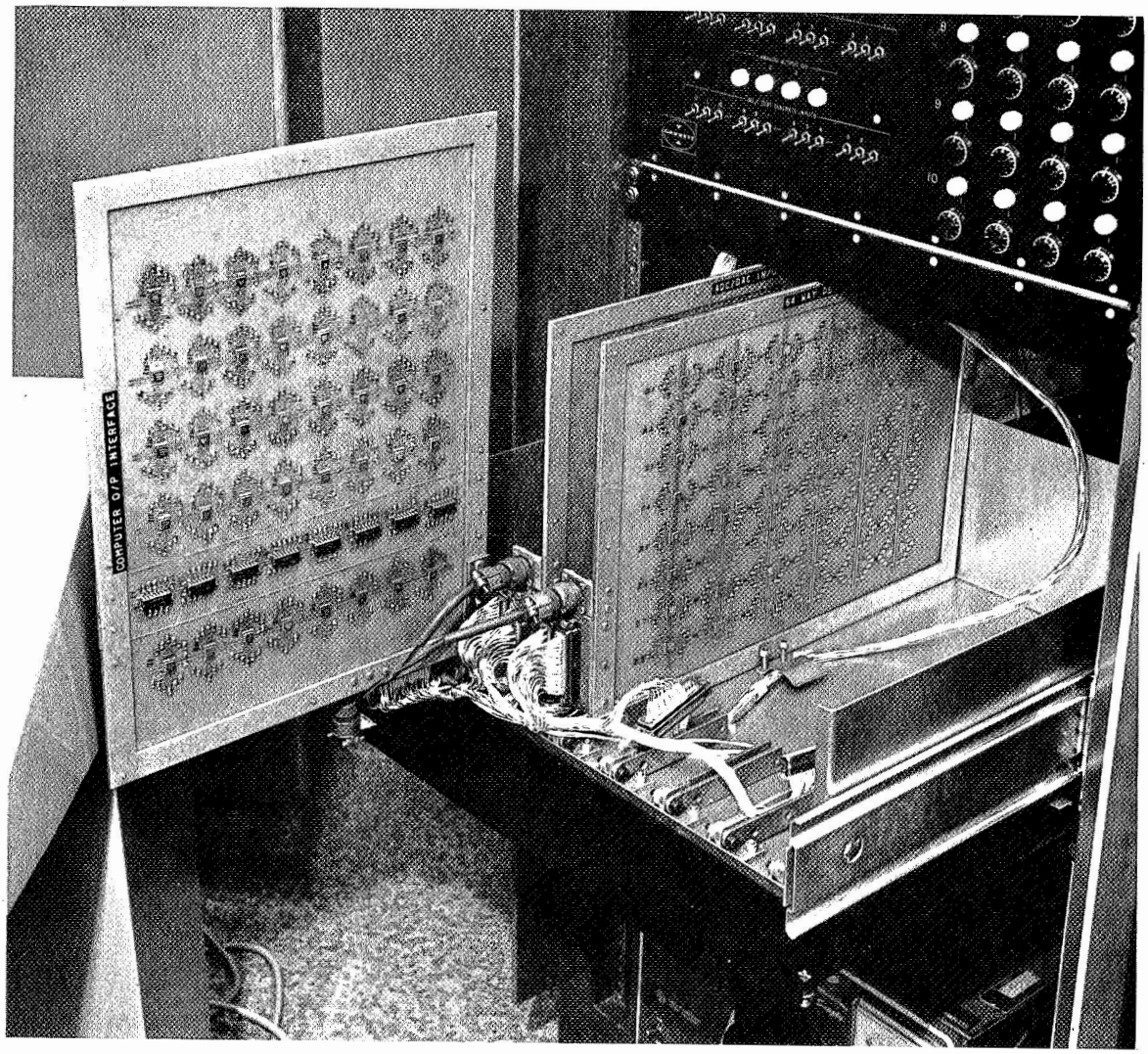
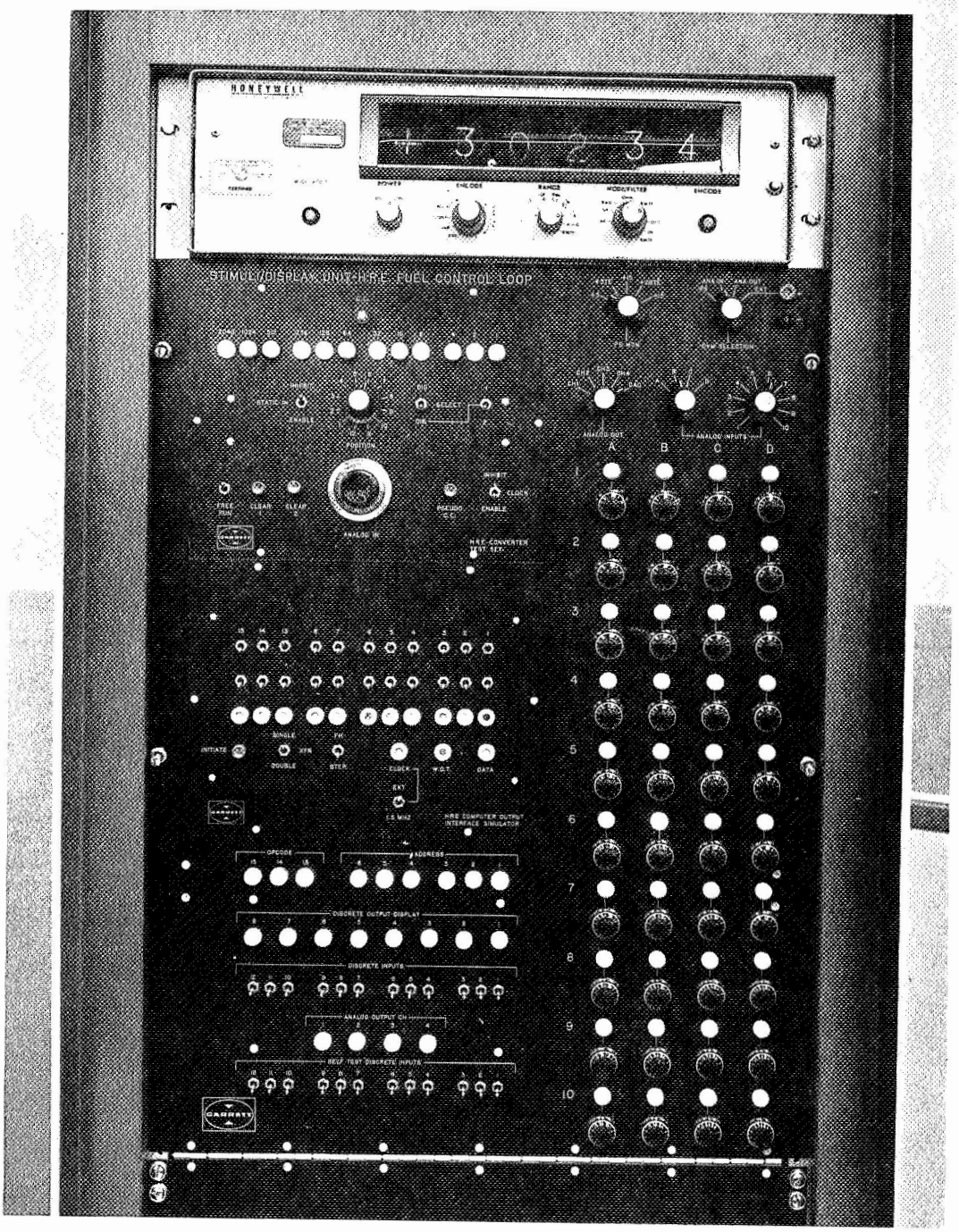


Figure 6.5-2. Stimuli/Display Hardware F-9389



F-9386

Figure 6.5-3. Digital Interface Hardware



F-9385

Figure 6.5-4. Stimuli/Display Facilities

With the facilities shown it is possible to check the operation of the fuel control system in all operating modes by single-stepping a control program using the computer simulator, and/or running the system with the computer and observing the displays.

The voltmeter facilities are also available to the temperature control loop by switch selection.

7.0 FUTURE ACTION

7.1 ANALYSES

7.1.1 Temperature and Fuel Control

Simulation studies that will include the hydrogen turbopump and the fuel injectors are continuing. Some further refinement of the heat exchanger simulation will take place. The complete system simulation will be integrated and system perturbation studies will be initiated.

7.1.2 Static Error

The system static error analysis was delayed but is expected to start early in the next report period.

7.2 SYSTEM STUDY

Although the failure modes analysis was initiated during the past period, the material has been withheld and will be presented in the fifth TDR as a complete subject.

7.3 HARDWARE

7.3.1 Computer

Engine control programs will be assembled and tested on the computer. Diagnostics and executive control routines will be written. The computer will be coupled to the breadboard equipment and the interface will be thoroughly tested. Several engineering programs will be written to facilitate testing.

7.3.2 Breadboard Activity

All final breadboard sections should be completed and tested. System integration will be complete with the possible exception of the power supply and monitoring circuits. Breadboard control system functional testing will be initiated.

APPENDIX A

ANALOG SIMULATION DETAILS

APPENDIX A

ANALOG SIMULATION DETAILS

This appendix describes the present status of the simulator in the form of wiring diagrams and working documentation. The amplifier assignment documents represent a definitive description with complete quantitative setup data.

A description of changes which have been implemented since the third TDR is included. Evolutionary changes that are presently foreseen are outlined briefly.

The changes which the simulator has undergone fall into two categories: internal changes in the wiring configuration which do not theoretically change the results of the simulation; and external changes which modify the model and, therefore, modify the results of the simulator.

The only external change in the simulator was the inclusion of a larger line between the outershell outlet manifold and the main fuel plenum, line 8. Rather than augment this change with paper calculations of the new initial conditions, the pipe was simply installed and the valve areas were adjusted to provide the correct flows. The new initial conditions were then read from the computer. Future external changes will include more accurately represented valves, new heat exchanger models, and modifications to update the configurations of the lines.

The internal changes include (1) new scaling, e.g., both pressures and temperatures are scaled to 2000 rather than 1100 and 1700 as originally done; (2) noise reduction (all trunk lines are fed into high input impedance amplifiers, and in general high currents are avoided in the trunks; (3) all square root generators have been replaced with double-ended square root generators which are capable of accepting both positive and negative input sign signals; (4) any manifold which previously used an integrator and two inverting amplifiers is now simulated with just one amplifier. This list of internal changes is incomplete, but it does give a representative sample. The new wiring diagram and the associated paperwork is included in this appendix.

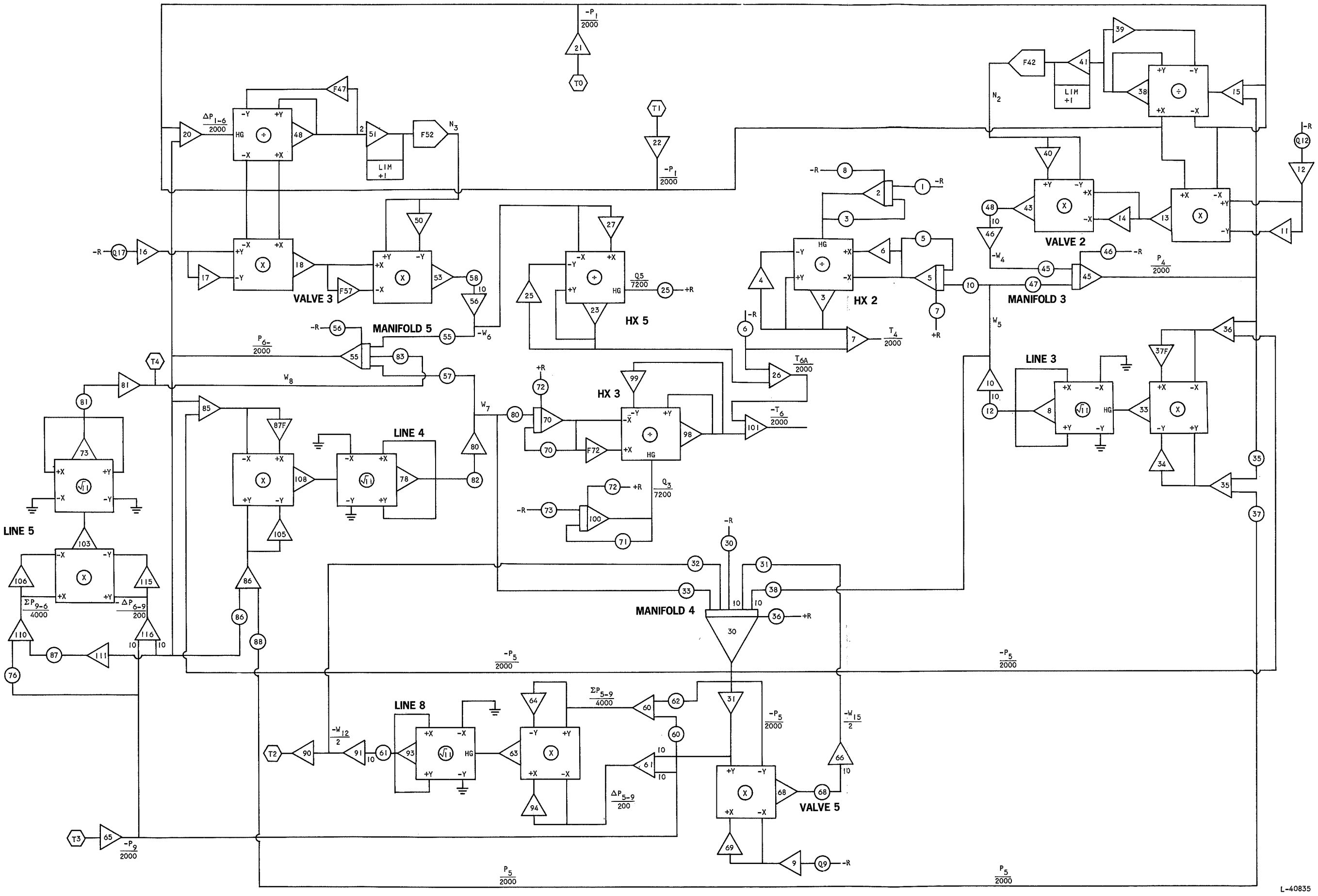


Figure A-1. HRE Fuel System Control Innerbody

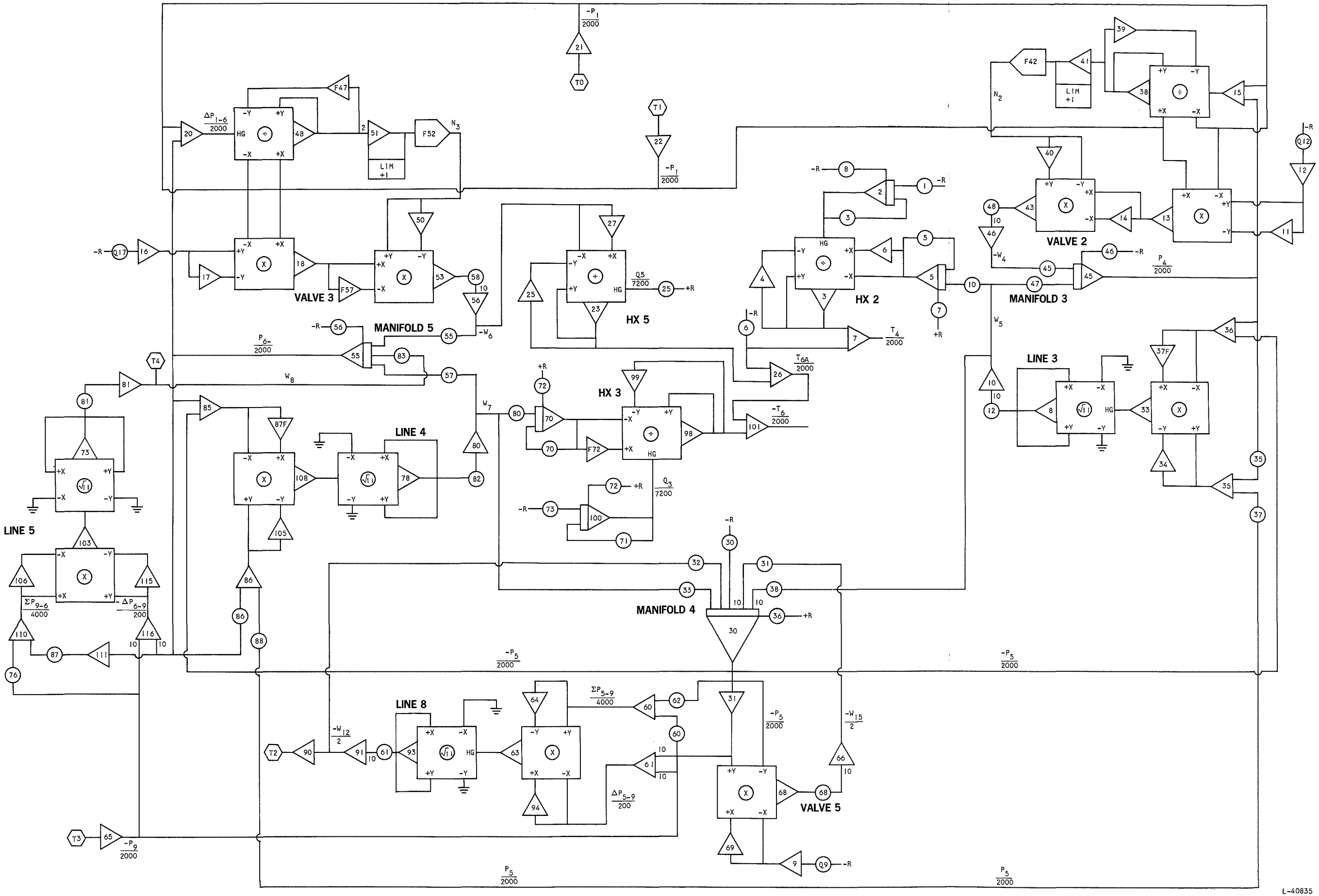


Figure A-2. HRE Fuel System Control Outerbody

EAI 680 AMPLIFIER ASSIGNMENT SHEET (A00-A59)

PROBLEM HRE Fuel System PROJECT# HRE

PROGRAMMER D.W./J.F.D. CONSOLE B DATE

AMP	USE	OUTPUT VARIABLE		ST CHECK DERIVATIVE	steady state CHECK VALUE
0					
1					
2	∫	$\dot{Q}_2/7200$	HX2	0	4565
3	M		HX2		5258
4	INV		HX2		5258
5	∫	$-W_5$	HX2	0	8700
6	INV		HX2		8700
7	Σ	$+T_4/2000$	HX2		5758
8	M		L3		1658
9	INV	$+\Delta V_5$	V5		7466
10	INV	$+W_5$	L3		+8700
11	INV		V2		5746
12	INV	$+10\Delta V_2$	V2		5746
13	M	$-\Delta V_2 P_1/200$	V2		3170
14	INV		V2		3170
15	Σ	$+\Delta P_{1-4}/2000$	V2		2086
16	INV	$+10\Delta V_3$	V3		6085
17	INV		V3		6085
18	M	$\Delta V_3 P_1/200$	V3		3355
19					
20	Σ	$\Delta P_{1-6}/2000$	V3		2260
21	INV	$-P_1/2000$	TP		+5500
22	INV	$+P/2000$	TP		+5500
23	M		HX5		-1949
24					
25	INV		HX5		+1949
26	Σ	$T_{6A}/2000$	HX5		+2449
27	INV		HX5		+9302
28					
29					

AMP	USE	OUTPUT VARIABLE		ST CHECK DERIVATIVE	steady state CHECK VALUE
30	∫	$-P_5/2000$	M4	0	2500
31	INV	$+P_5/2000$	M4		2500
32					
33	M		L3		10275
34	INV		L3		+2962
35	Σ	$-\Sigma P_{4-5}/2000$	L3		-2962
36	Σ	$-\Delta P_{4-5}/2000$	L3		-0925
37					
38	M		V2		-3770
39	INV		V2		+3770
40	INV		V2		-9826
41	INV		V2		+7540
42					
43	M		V2		+3118
44					
45	∫	$P_4/2000$	M3	0	+3424
46	INV	$-W_4$			-8700
47					
48	M		V3		-4094
49					
50	INV		V3		-9953
51	INV	$2\Delta P_{1-6}/P_1$	V3		+8890
52					
53	M		V3		+3333
54					
55	∫	$P_6/2000$	M5	0	+3246
56	INV	$-W_6$	V3		-9300
57					
58					
59					

EAI 680 AMPLIFIER ASSIGNMENT SHEET (A60-A119)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE B DATE _____

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	ST CHECK VALUE	Steady state CHECK VALUE
60	Σ	$\Sigma P5\text{-}9/1000$ L8		+2500	
61	Σ	$-\Delta P5\text{-}9/200$ L8		+0005	
62					
63	M	L8		+0002	
64	INV	L8		-2500	
65	INV	L8		-2500	
66	INV	$-W15/2$ V5		-7440	
67					
68	M	V5		+1860	
69	INV	V5		-7440	
70	S	-W7 HX3	0	-8710	
71					
72					
73	M	L5		-4628	
74					
75					
76					
77					
78	M	L4		-1467	
79					
80	INV	+W7 L4		+8710	
81	INV	+W8 L5		+0587	
82					
83					
84					
85	Σ	$-\Delta P6\text{-}5/1000$ L4		-0747	
86	Σ	$-\Sigma P6\text{-}5/1000$ L4		-2873	
87					
88					
89					

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	ST CHECK VALUE	Steady state CHECK VALUE
90	INV	$+W12/2$ L8		-0230	
91	INV	$-W12/2$ L8		+0230	
92					
93	M	L8		-0113	
94	INV	L8		-0005	
95					
96					
97					
98	M	HX3		-3657	
99	INV	$+\Delta T6/2000$ HX3		+3657	
100	S	$+Q3/7200$ HX3	0	+3187	
101	INV	$-T6/2000$ HX3		-6105	
102					
103	M	L5		+1142	
104					
105	INV	L4			
106	INV	$-\Sigma P9\text{-}6/4000$ L5		+2873	
107					
108	M	L4		+0215	
109					
110	Σ	$\Sigma P9\text{-}6/2000$ L5		+2873	
111	INV	$-P6/2000$ L5		-3246	
112					
113					
114					
115	INV	L5		+7460	
116	Σ	$\Delta P6\text{-}9/200$ L5		-7460	
117					
118					
119					

EAI 680 POTENTIOMETER ASSIGNMENT SHEET (P00-P59)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE B DATE _____

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
0			
1			0152
2			
3			0333
4			
5			9999
6			0500
7			8700
8			4560
9			
10			9999
11			
12			5245
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			1813
26			
27			
28			
29			

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
30			1383
31			9220
32			0922
33			4610
34			
35			5000
36			2500
37			5000
38			0462
39			
40			
41			
42			
43			5000
44			
45			0404
46			3428
47			0404
48			2790
49			
50			
51			
52			
53			
54			
55			1635
56			3250
57			1635
58			2790
59			

EAI 680 POTENTIOMETER ASSIGNMENT SHEET (P60-P119)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE 13 DATE _____

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
60			5000
61			2030
62			5000
63			1000
64			
65			
66			2000
67			
68			4000
69			
70			5840
71			0333
72			8700
73			0906
74			
75			
76			
77			3187
78			
79			
80			8840
81			1268
82			5935
83			1635
84			
85			
86			5000
87			5000
88			5000
89			

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
90			
91			
92			
93			
94			
95			
96			
97			
98			
99			
100			
101			
102			
103			
104			
105			
106			
107			
108			
109			
110			
111			
112			
113			
114			
115			
116			
117			
118			
119			

EAI 680 NONLINEAR COMPONENT ASSIGNMENT SHEET

(MULTIPLIERS, DFG's, LIMITERS, AND HAND SET POTS)

PROBLEM _____ PROJECT# _____

PROGRAMMER _____ CONSOLE B DATE _____

HAND POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
2			
4			
7			
9			
12	VALVE 2		5733
14			

HAND POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
17	VALVE 3		6113
19			
22			
24			
27			
29			

LIMITER	AMP	LIMITED VARIABLE	CHECK SETTINGS +	CHECK SETTINGS −	RUN SETTINGS +	RUN SETTINGS −
1						
11						
21						
31						
41		$2\,\Delta P_{1\text{-}4}/P_1$			+1	0
51		$2\,\Delta P_{1\text{-}6}/P_1$			+1	0
61						
71						
81						
91						
101						
111						

VDFG	USE	OUTPUT VARIABLE	CHECK VALUE
32			
42	DFG	N-function N_2 V_2	+9826
52	DFG	" N_3 V_2	+9951
62	INV	HX_3	-0020
72			
82			
92			
102			
112			

VDFG	USE	OUTPUT VARIABLE	CHECK VALUE
37	INV	L_3	+0925
47	INV	V_3	+4096
57	INV	V_3	+3354
67			
77			
87	INV	L_4	+0748
97			
107			
117			

MULT	USE	MULT	USE	MULT	USE	MULT	USE	FDFG	TYPE	USE	FDFG	TYPE	USE	FDFG	TYPE	USE
3		33		63		93		32			62			92		
8		38		68		98		37			67			97		
13		43		73		103		42			72			102		
18		48		78		108		47			77			107		
23		53		83		113		52			82			112		
28		58		88		118		57			87			117		

EAI 680 AMPLIFIER ASSIGNMENT SHEET (A00-A59)

PROBLEM HRG Fuel System PROJECT# HRE

PROGRAMMER D.W./J.F.D. CONSOLE C. DATE

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	ST CHECK VALUE	steady state CHECK VALUE
0	∫	$+Q_7/7200$ HX4	0	+3100	
1	Σ	$-\Sigma P_{8-9}/4000$ L7		-2537	
2	Σ	$+\Delta P_{8-9}/200$ L7		+0715	
3	M	L7		-0180	
4	INV	L7		-0715	
5	∫	$-P_8/2000$ M7	0	-2573	
6	INV	$+P_8/2000$ M7		+2573	
7	INV	$-W_{11}$ L7		-4200	
8	M	L7		+1341	
9	INV	L7		+2538	
* 10	∫	$+Q_1/7200$ HX1	0	+4678	
11					
12	Σ	$\Delta P_{1-2}/2000$ V1		+1188	
13	M	V1		+2160	
14					
15	∫	$-P_1/2000$ TP	0	+5500	
16	INV	$P_1/2000$ TP		-5500	
17					
18	M	$+A_{V4}N_4P_1/200$ V4		+1508	
19					
20	∫	$+P_7/2000$ M6		+4580	
21	INV	$-W_9$ V4		-4200	
22	INV	V4		-7690	
23	M	V4		-1960	
24					
25	INV	V4		+1961	
26	INV	$-10A_{V4}$ V4		-3584	
27	INV	$+0A_{V4}$ V4		+3564	
28					
29					

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	ST CHECK VALUE	steady state CHECK VALUE
30	∫	$-W_{10}$ HX4	0	-4200	
31	Σ	$T_7/2000$ HX4		+7943	
32	INV	HX4		+4200	
33	M	HX4		-7443	7380
34	INV	HX4		+7443	
35	∫	$-W_2$ HX1	0	-7800	***
36	Σ	$+T_2/2000$ HX1		+6510	****
37	INV	HX1		+6012	
38	M	$-T_2/2000$ HX1		-6012	***
39	INV	V1		-6018	
40	INV	$+0A_{V1}$ V1		+6018	
41	INV	$-2\Delta P_{1-7}/P_1$ V1		-4310	
42					
43	M	V1		-3314	
44					
45	∫	$P_2/2000$ M1	0	+4313	
46	INV	$-W_1$ V1		-7800	
47					
48	M	$A_{V1}N_1P_1/200$ V1		+2785	
49					
50	Σ	$+\Delta P_{1-7}/2000$ V4		+0920	
51	INV	$2\Delta P_{1-7}/P_1$ V4		+3300	
52					
53	M	V4		-1647	
54					
55					
56					
57					
58					
59					

* no more used in temp. control

** time integrator

*** free

**** time system

EAI 680 AMPLIFIER ASSIGNMENT SHEET (A60-A119)

PROBLEM _____ PROJECT# _____

PROGRAMMER _____ CONSOLE C DATE _____

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	ST CHECK VALUE (Steady State)
60				
61	Σ	$-\Sigma P_{3-9}/2000$	L_2	-2753
62	INV		L_2	-0465
63	M		L_2	+1132
64	INV	$+P_3/2000$	M_2	+2966
65	∫	$-P_3/2000$	M_2 0	+2966
66	INV	$-W_3$	L_2	-7800
67	INV		HX1	+7800
68	M		L_2	-0128
69	INV		L_2	+2733
70	INV	W_2		+7800
71	Σ	$-\Sigma P_{2-3}/4000$	L_1	-3640
72	INV		L_1	+3040
73	M		L_1	-2218
74				
75				
76	Σ	$-\Delta P_{2-3}/2000$	L_1	-1348
77	INV		V_1	-8430
78	M		L_1	+0492
79				
80				
81	Σ	$-\Delta P_{7-8}/2000$		-2008
82				
83				
84				
85				
86	Σ	$-\Sigma P_{1-8}/4000$	L_6	-3577
87				
88				
89				

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	ST CHECK VALUE (Steady State)
90				
91				
92				
93				
94	Σ	$+\Delta P_{3-9}/2000$	L_2	+0465
95				
96				
97				
98				
99				
100	∫	$P_9/2000$	M_8 0	+2500
101				
102				
103	M		L_6	-2680
104				
105				
106	INV	W_{10}	L_6	+4200
107				
108	M		L_6	+0718
109				
110				
111				
112				
113				
114				
115				
116				
117				
118				
119				

EAI 680 POTENTIOMETER ASSIGNMENT SHEET (P00-P59)

PROBLEM _____ PROJECT# _____

PROGRAMMER _____ CONSOLE C DATE _____

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
0	New Value: 7500		0104
1			5000
2	6925		0333
3			5000
4			
5			1704
6			3121
7			1704
8			8110
9			
10	Bics 3608	free	0156
11		free	4675
12		free	0333
13			2572
14			
15	1525		
16			
17	0263		
18			5500
19			
20			0333
21			4596
22			0333
23			2790
24			
25			
26			1257
27			
28			1257
29			

1257

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
30	5950		4650
31	BIAS 4200		0800
32	7500		4650
33			3606
34			
35		free	9040
36		free	7800
37		free	9040
38	2155		
39			
40			1267
41			9810
42			1267
43	IC (P9/2000		2500
44			
45			0240
46			4323
47			0240
48			2790
49			
50	Bics 3591 recorder		
51			
52			
53			
54			
55			
56	0500		
57			
58			
59			

EAI 680 POTENTIOMETER ASSIGNMENT SHEET (P60-P119)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE C DATE _____

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
60	5315		4200
61			5000
62	BIAS SCALE		7885
63			5000
64			
65			8110
66			0811
67			1622
68			6875
69			
70			2967
71			5000
72			3508
73			5000
74			
75			
76	2921		
77			
78			1563
79			
80			
81			3641
82			
83			0215
84			
85			
86			5000
87			
88			5000
89			

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
90			
91			
92			
93			
94			
95			
96			
97			
98			
99			
100			
101			
102			
103			
104			
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116			
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118			
119			

EAI 680 NONLINEAR COMPONENT ASSIGNMENT SHEET

(MULTIPLIERS, DFG's, LIMITERS, AND HAND SET POTS)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE C DATE _____

HAND POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
2			3641
4			
⑦	Kd (Temp control)		
⑨	GAIN (Temp Contr)		
12	VALVE1		6073
14			

HAND POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
17			2500
19	VALVE4		
22			
24			
27			
29			

LIMITER	AMP	LIMITED VARIABLE	CHECK SETTINGS +	CHECK SETTINGS −	RUN SETTINGS +	RUN SETTINGS −
1						
11						
21						
31						
41		ΔP1-4 / P1			0	-10
51		ΔP1-6 / P1			+1	0
61						
71						
81						
91						
101						
111						

VDFG	USE	OUTPUT VARIABLE	CHECK VALUE
32	INV	M8	-0588
42	INV	V1	+2160
52			
62			
72	DFG	V4	F7700
82	INV	L6	+2008
92			
102			
112			

VDFG	USE	OUTPUT VARIABLE	CHECK VALUE
37	INV	M8	0230
47			
57	INV	V4	+1674
67	DFG	V1	+8430
77	INV	V1	+3395
87	INV	L6	+3579
97			
107			
117			

MULT	USE	MULT	USE	MULT	USE	MULT	USE	FDFG	TYPE	USE	FDFG	TYPE	USE	FDFG	TYPE	USE
3		33		63		93		32			62			92		
8		38		68		98		37			67			97		
13		43		73		103		42			72			102		
18		48		78		108		47			77			107		
23		53		83		113		52			82			112		
28		58		88		118		57			87			117		

APPENDIX B

MATHEMATICAL MODELS - FREQUENCY RESPONSE PERIPHERALS

APPENDIX B

MATHEMATICAL MODEL STUDIES - FREQUENCY RESPONSE PERIPHERALS

INTRODUCTION

This appendix describes the function of the frequency response peripheral equipment. This equipment is used to automatically produce Bode plots for one decade of frequency, and is essential due to the complexity of the system and the large amount of frequency response tests which are to be run.

The accuracy of the device depends on the accuracy of two peak detector circuits, and the accuracy of the log-function generators. Accuracy of these elements is estimated at ±1 percent.

COMMENTS ON PERIPHERAL MECHANIZATION

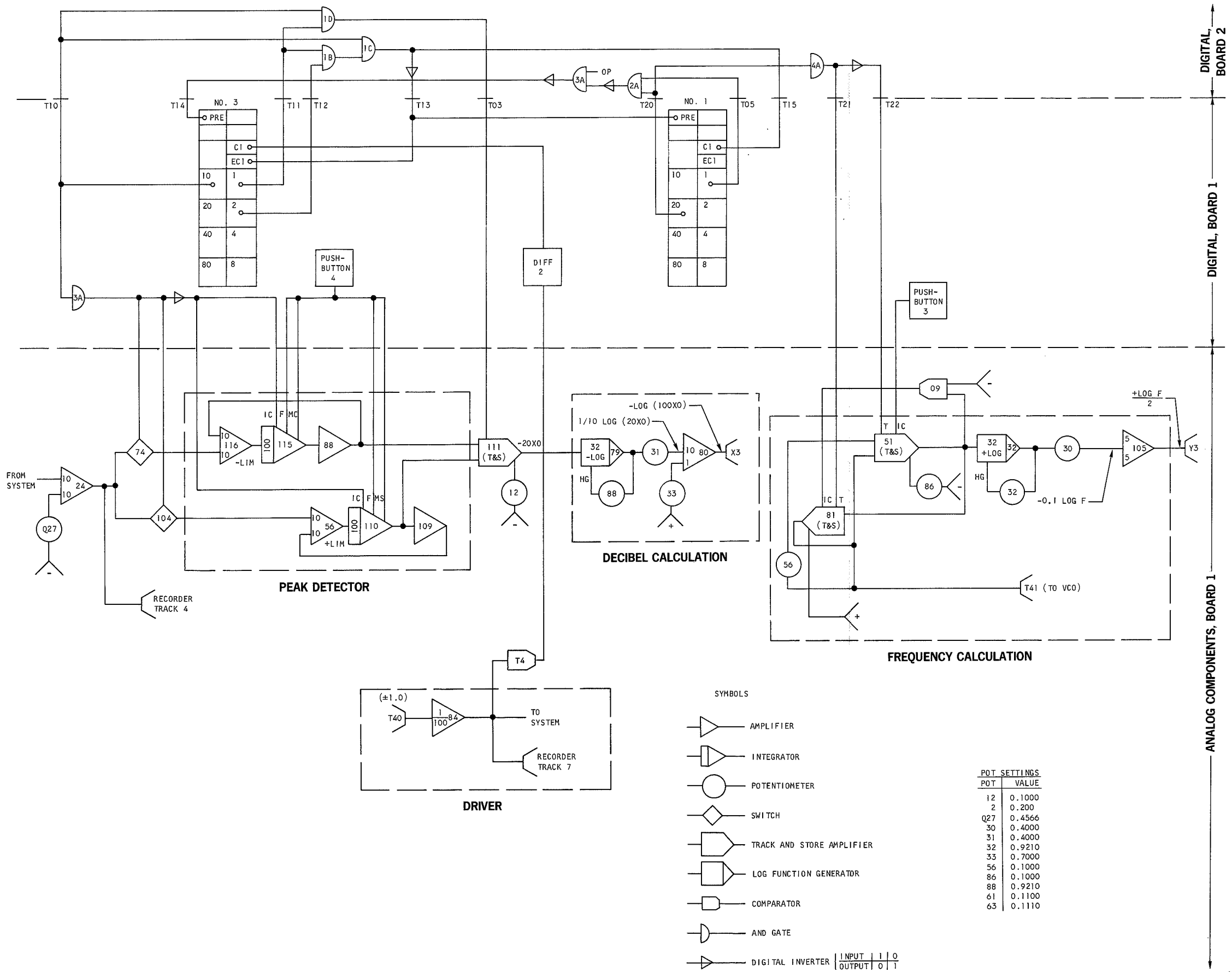
The function of the frequency response peripherals was (1) to control the frequency of the input oscillation, (2) to measure amplitude of the response signal, (3) to calculate the log of the gain, and (4) to plot the results.

The wiring diagram for this device is shown in Figure B-1. The function of the device will be explained by first discussing the functions of the individual components (e.g., peak detector, decibel calculation) and then the functions of the overall system.

Component Discussion

The peak detector has two channels, one for sensing the positive signal amplitude and one for sensing the negative signal amplitude. The two error sensing amplifiers, No. 56 and 116, are zero limiters. Amplifier 56 can have only positive output values, and therefore will only allow the value of integrator 115 to decrease, i.e., to follow the negative peaks of the input signals. Since the open-loop gain of the detectors is high, the detectors will follow the inputs quite closely while the inputs are increasing. Integrator 115 will, for instance, follow an increasing positive signal (from amplifier 25) with a time constant of 1/1000 sec, which corresponds to a bandwidth of about 160 Hz. Since the frequency of the input never exceeds 10 Hz, the peak detector will find the peak amplitude with a high degree of accuracy. The peak values are summed into track and store amplifier 111. The output of amplifier 111 is therefore equal to the peak-to-peak amplitude of the output of amplifier 24.

The decibel calculation relates its input to an output proportional to the gain of the system in decibels. The output of amplifier 79 is equal to $+1/4 \log_{10}(\text{input})$. Since no analog variable can have a value greater than 1, the output of amplifier 79 will always be negative. If the input to the log function was 20 X_o, the output of pot 31 will be 0.1 log 20 X_o. Multiplying this signal by 10 and adding the log of 5 to it produces the final



POT SETTINGS

POT	VALUE
12	0.1000
2	0.200
Q27	0.4566
30	0.4000
31	0.4000
32	0.9210
33	0.7000
56	0.1000
86	0.1000
88	0.9210
61	0.1100
63	0.1110

Figure B-1. HRE Bode Plot Peripherals Board No. 1, Computer A

output, -log (100 X_o). Since the input to the system (the forcing function) has an amplitude of 0.01, the output of amplifier 80 is also equivalent to -log (Xo/Xi). If Xo = Xi, the output will be zero which corresponds to zero decibels on the X-Y recorder. If Xo = Xi/2 = 0.005, then the output will be -log 0.5 = 0.3. Since one computer unit is equivalent to 10 v, this is 3 v. Making 3 v correspond to -6 db on the X-Y plotter establishes the correct scale for recording the magnitude of the output in decibels.

The frequency calculation produces a signal which varies from 0.1 to 1.0 (or from 1 v to 10 v), which is proportional to frequency for one decade of change. This signal is produced by amplifiers 51 and 81. The initial condition for amplifier 51 is 0.1. This value is held by amplifier 81. The input to amplifier 51 is now 0.1 + 0.1 x pot 56. If pot 56 is set to 0.1, then the input to 51 is 0.11. The next time that amplifier 51 goes into track mode, its value will become 0.11. Amplifier 51 then goes into store mode, 81 gees into track, and then store, and the new input to 51 is 0.121. The effect of this circuit is to increase the voltage of 51 by a constant factor each time the truck and store cycle is repeated. Since each step multiplies frequency by a constant value, the distance between steps of log frequency will be constant. The output of pot 30 is -0.1 log f, and hence is always psoitive. The output of amplifier 105 is 1/2 log f, and therefore will vary from -0.5 for f = 0.1 to 0 for f = 1.0.

System Discussion

The operation of the system is synchronized by comparator 74. It signals a positive value of the system input by emitting a logic 1, and negative values by a logic zero. Its signal is fed to differentiator 2, which emits a blip every time comparator 74 becomes 1. This blip tells the binary-coded decimal counter No. 3 to increase its count by one. When this counter reads 10 or more, and-gate 3A closes switches 74 and 104 and takes integrators 110 and 115 out of IC mode. When the count on No. 3 reaches 11, and-gate ID tells ta track and store amplifier 111 to track. When No. 3 reaches 13, and-gate IC tells counter No. 3 to stop counting, and counter No. 1 to start counting. Counter No. 1 counts continuously, giving the system enough time to plot the data (control of the X-Y plotter is not shown in Figure B-1). When counter No. 1 reaches 20(it counts continuously), it increments the frequency through and-gate 4A. When counter No. 1 reaches 21, counter No. 3 resets and resumes counting; counter No. 1 then resets and stops counting.

APPENDIX C

MATHEMATIC MODEL STUDIES
COMPENSATION CALCULATIONS

APPENDIX C

MATHEMATICAL MODEL STUDIES
COMPENSATION CALCULATIONS

This appendix includes the calculations for the first-order and second-order digital compensators, listings of the programs used to calculate numerical values, and sample results.

1ST ORDER DIGITAL COMPENSATION

$$\frac{E_o}{E_i} = \frac{S + \alpha}{S + \beta}\left(\frac{\beta}{\alpha}\right) = \frac{\frac{1}{\alpha} S + 1}{\frac{1}{\beta} S + 1}$$

$$\frac{\dot{E}_o}{\beta} + E_o = \frac{\dot{E}_i}{\alpha} + E_i$$

$$\frac{E_o}{\beta T} - \frac{Z^{-1} E_o}{\beta T} + E_o = \frac{E_i}{\alpha T} - \frac{Z^{-1} E_i}{\alpha T} + E_i$$

$$E_o (Z)\left(1 + \frac{1}{\beta T} - \frac{Z^{-1}}{\beta T}\right) = E_i \left(1 + \frac{1}{\alpha T} - \frac{Z^{-1}}{\alpha T}\right)$$

$$\frac{E_o}{E_i} = \frac{1 + \frac{1}{\alpha T} - \frac{Z^{-1}}{\alpha T}}{1 + \frac{1}{\beta T} - \frac{Z^{-1}}{\beta T}} = \frac{\beta t}{\alpha t}\left[\frac{(1 + \alpha T) Z - 1}{(1 + \beta T) Z - 1}\right]$$

Zero at $+ \frac{1}{1 + \alpha T}$

Pole at $+ \frac{1}{1 + \beta T}$

$\beta \rightarrow \infty$, Pole $\rightarrow 0$

$\alpha \rightarrow 0$, Zero $\rightarrow 1$

$Z \rightarrow 1$, $E_o/E_i \rightarrow 1$

$$\frac{E_o}{E_i} = G_c(Z) = \frac{\beta}{\alpha}\ \frac{(1 + \alpha T)Z - 1}{(1 + \beta B)Z - 1}$$

$$\frac{1-G_c}{G_c} = \frac{1 - \frac{\left[(1 + \alpha T)Z - 1\right]}{\alpha\left[(1 + \beta T)Z - 1\right]}}{\frac{\beta\left[(1 + \alpha T)Z - 1\right]}{\alpha\left[(1 + \beta T)Z - 1\right]}}$$

$$= \frac{\alpha Z - \alpha - \beta Z + \beta}{\beta\left[(1 + \alpha T)Z - 1\right]}$$

$$= \frac{Z(\alpha-\beta) - (\alpha-\beta)}{\beta\left[(1+\alpha T)Z - 1\right]}$$

$$= \frac{(\alpha-\beta)(1 - Z^{-1})}{\beta\left[1+\alpha T\right]\left[1 - \frac{1}{1+\alpha T} Z^{-1}\right]}$$

$$Z\left[\frac{H(S)}{S}\right] = \frac{(\alpha-\beta)}{\beta\left[1+\alpha T\right]\left[1 - \frac{1}{1+\alpha T} Z^{-1}\right]}$$

$$\frac{H(S)}{S} = \frac{\alpha-\beta}{\beta(1+\alpha T)} \frac{1}{S + \frac{\log(1+\alpha T)}{T}}$$

$$H(S) = \frac{\alpha-\beta}{\beta(1+\alpha T)} \frac{S}{S + \frac{\log(1+\alpha T)}{T}}$$

NOTE: $\beta > \alpha$

$$H(S) = - \frac{B-\alpha}{\beta(1+\alpha T)} \frac{S}{S + \frac{\log(1+\alpha T)}{T}}$$

$$\frac{E_o}{E_i} = K \frac{SCR}{1+SCR}$$

$$= \frac{KS}{S + \frac{1}{CR}}$$

$$RC = \frac{T}{\log(1+\alpha T)}$$

$$K = \frac{\beta-\alpha}{\beta(1+\alpha T)}$$

$$K = \frac{\beta-\alpha}{\beta(1+\alpha T)} = \frac{1-\frac{\alpha}{\beta}}{1+\alpha T}$$

$$\beta \to \infty,\ K \to \frac{1}{1+\alpha T}$$

$$\alpha \to 0,\ K \to 1$$

$$RC = \frac{T}{\log\ (1+\alpha T)}$$

$$\alpha \to 0,\ RC \to \infty$$

$$T \to 0,\ RC \to \frac{1}{\alpha}$$

$$T = 0.025$$

$$\alpha < 1$$

2ND ORDER DIGITAL COMPENSATION

$$Gc(Z) = \frac{(Z-\alpha)(Z-\gamma)(1-\beta)(1-\delta)}{(Z-\beta)(Z-\delta)(1-\alpha)(1-\gamma)}$$

$$\frac{1-G_c}{G_c} = \frac{(Z-\beta)(Z-\delta)(1-\alpha)(1-\gamma) - (Z-\alpha)(Z-\gamma)(1-\beta)(1-\delta)}{(Z-\alpha)(Z-\gamma)(1-\beta)(1-\delta)}$$

$$\text{Numerator} = Z^2(\alpha\gamma - \beta\delta - \alpha + \beta - \gamma + \delta)$$

$$- Z(\alpha\beta\gamma - \alpha\beta\delta + \alpha\gamma\delta - \beta\gamma\delta - \alpha + \beta - \gamma + \delta) + \ldots$$

$$\text{Numerator} = Z^2\left[(1-\alpha-\gamma+\alpha\gamma) - (1-\beta-\delta+\beta\delta)\right]$$

$$-Z\left[(\delta+\beta)(1-\alpha-\gamma+\alpha\gamma) - (\alpha+\gamma)(1-\beta-\delta+\beta\delta)\right]$$

$$+\beta\delta(1-\alpha)(1-\gamma) - \alpha\gamma(1-\beta)(1-\delta)$$

$$= Z^2\left[\alpha\gamma - \beta\delta - \alpha + \beta - \gamma + \delta\right]$$

$$-Z\left[\alpha\beta\gamma - \alpha\beta\delta + \alpha\gamma\delta - \beta\gamma\delta - \alpha\ \beta - \gamma + \delta\right]$$

$$+\left[\beta\delta - \alpha\gamma - \alpha\beta\delta - \gamma\beta\delta + \alpha\gamma B + \alpha\gamma\delta\right]$$

SYNTH DIVIDE

$$\frac{\alpha\gamma - \beta\delta - \alpha + \beta - \gamma + \delta}{\alpha\gamma - \beta\delta - \alpha + \beta - \gamma + \delta}$$

$$\begin{array}{r} -\alpha\beta\gamma + \alpha\beta\delta - \alpha\gamma\delta + \beta\gamma\delta + \alpha - \beta + \gamma - \delta \\ \alpha\gamma - \beta\delta \qquad\qquad\qquad\qquad - \alpha + \beta - \gamma + \delta \\ \hline -\alpha\beta\gamma + \alpha\beta\delta - \alpha\gamma\delta + \beta\gamma\delta + \alpha\gamma - \beta\delta \end{array}$$

$$\beta\delta - \alpha\gamma - \alpha\beta\delta - \gamma\beta\delta + \alpha\gamma\beta + \alpha\gamma\delta$$

$$\text{Numerator} = (Z - 1)\left[(\alpha\gamma - \beta\delta - \alpha + \beta - \gamma + \delta)Z - (\alpha\beta\gamma + \gamma\beta\delta - \alpha\beta\gamma - \alpha\gamma\delta - \beta\delta + \alpha\gamma)\right]'$$

$$= (Z - 1)\left[\{(\alpha - \beta)(\gamma - 1) + (\gamma - \delta)(\beta - 1)\}Z - \{\alpha\gamma(1 - \beta - \delta) - \beta\delta(1 - \alpha - \gamma)\}\right]$$

$$= (Z - 1)\left[\{(\alpha - \beta)(\gamma - 1) + (\gamma - \delta)(\beta - 1)\}Z - \{\gamma(\alpha - \beta)(1 - \delta) + \beta(\gamma - \delta)(1 - \alpha)\}\right]$$

$$= (Z - 1)\left[\{\alpha - \beta)(\gamma - 1) + (\gamma - \delta)(\beta - 1)\}Z - \{\delta(\alpha - \beta)(\gamma - 1) + \alpha(\gamma - \delta)(\beta - 1)\}\right]$$

$$\frac{1 - Gc}{Gc} = \frac{(1-Z^{-1})\left[\{(\alpha-\beta)(\gamma-1) + (\gamma-\delta)(\beta-1)\} - \{\delta(\alpha-\beta)(\gamma-1) + \alpha(\gamma-\delta)(\beta-1)\}Z^{-1}\right]}{(1-\alpha Z^{-1})(1-\gamma Z^{-1})(1-\beta)(1-\delta)}$$

$$Z\left(\frac{H(S)}{S}\right) = \frac{K_1}{(1-\alpha Z^{-1})} + \frac{K_2}{(1-\gamma Z^{-1})}$$

$$K_1 = \frac{\left[\{(\alpha-\beta)(\gamma-1)\} - \frac{\delta}{\alpha}(\alpha-\beta)(\gamma-1)\right]}{\left(1-\frac{\gamma}{\alpha}\right)(1-\beta)(1-\delta)}$$

$$= \frac{(\alpha-\beta)(\gamma-1)(\alpha-\delta)}{(\alpha-\gamma)(1-\beta)(1-\delta)}$$

$$K_2 = \frac{\left[\{(\alpha-\beta)(\gamma-1) + (\gamma-\delta)(\beta-1)\} - \{\frac{\delta}{\gamma}(\alpha-\beta)(\gamma-1) + \frac{\alpha}{\gamma}(\gamma-\delta)(\beta-1)\}\right]}{(-\frac{\alpha}{\gamma})(1-\beta)(1-\delta)}$$

$$= \frac{(\alpha-\beta)(\gamma-1)(\gamma-\delta) + (\gamma-\delta)(\beta-1)(\gamma-\alpha)}{(\gamma-\alpha)(1-\beta)(1-\delta)}$$

$$= \frac{(\alpha-\beta)(\gamma-1)(\gamma-\delta)}{(\gamma-\alpha)(1-\beta)(1-\delta)} - \frac{(\gamma-\delta)}{(1-\delta)}$$

$$\frac{H(S)}{S} = \frac{K_1}{S + \frac{\ln\frac{1}{\alpha}}{T}} + \frac{K_2}{S + \frac{\ln\frac{1}{\gamma}}{T}}$$

$$H(S) = \frac{K_1 S}{S + \frac{\ln\frac{1}{\alpha}}{T}} + \frac{K_2 S}{S + \frac{\ln\frac{1}{\gamma}}{T}}$$

$$= \frac{(K_1 + K_2)S^2 + \left(K_1 \frac{\ln\frac{1}{\gamma}}{T} + K_2 \frac{\ln\frac{1}{\alpha}}{T}\right) S}{\left(S + \frac{\left(\ln\frac{1}{\alpha}\right)}{T}\right)\left(S + \frac{\left(\ln\frac{1}{\gamma}\right)}{T}\right)}$$

$$K_1 + K_2 = \frac{(\alpha-\beta)(\gamma-1)(\alpha-\delta)}{(\alpha-\gamma)(1-\beta)(1-\delta)} - \frac{(\alpha-\beta)(\gamma-1)(\gamma-\delta)}{(\alpha-\gamma)(1-\beta)(1-\gamma)} - \frac{\gamma-\delta}{1-\delta}$$

$$= \frac{(\alpha-\beta)(\gamma-1)}{(1-\beta)(1-\delta)} - \frac{(\gamma-\delta)}{1-\delta}$$

CIRCUIT: $\frac{Eo}{Ei} = \frac{KS(S+D)}{(S+E)(S+F)}$

FORMULAS

$$K_1 = \frac{(\alpha-\beta)(\gamma-1)(\alpha-\delta)}{(\alpha-\gamma)(1-\beta)(1-\delta)}$$

$$K_2 = -\frac{(\alpha-\beta)(\gamma-1)(\gamma-\delta)}{(\alpha-\gamma)(1-\beta)(1-\delta)} - \frac{(\gamma-\delta)}{(1-\delta)}$$

$$= -K_1 \frac{(\gamma-\delta)}{(\alpha-\delta)} - \frac{(\gamma-\delta)}{(1-\delta)}$$

$$= (\delta-\gamma)\left[\frac{K_1}{(\alpha-\delta)} + \frac{1}{(1-\delta)}\right]$$

$$K = K_1 + K_2$$

$$K/D = \frac{(K_1 + K_2)^2 T}{K_1 \ln\frac{1}{\gamma} + K_2 \ln\frac{1}{\alpha}}$$

$$EF = \frac{\ln\left(\frac{1}{\gamma}\right) \ln\left(\frac{1}{\alpha}\right)}{T^2}$$

$$E+F = \frac{\ln\left(\frac{1}{\alpha\gamma}\right)}{T}$$

0.249999		-0.926470	-60.324791	791.131837	69.718887
0.199999		-0.921568	-68.171432	918.475831	78.644653
0.149999		-0.916666	-78.430450	1082.650882	90.151993
0.099999		-0.911764	-93.134079	1314.042971	106.370697
0.049999		-0.906862	-118.819412	1709.612308	134.096893
-0.000000		-0.901960	-552.998536	8063.708997	579.467286
	-0.799999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.995370	-15.897510	29.272075	16.318733
0.899999		-0.990740	-17.625373	60.127166	18.481426
0.849999		-0.986110	-19.462070	92.746383	20.767765
0.799999		-0.981481	-21.421215	127.343643	23.192756
0.749999		-0.976851	-23.519096	164.174560	25.774303
0.699999		-1.125000	-26.289066	203.547485	28.534023
0.649999		-0.967593	-28.214550	245.839569	31.498344
0.599999		-0.962962	-30.866458	291.518372	34.700065
0.549999		-0.958333	-33.769409	341.174134	38.180519
0.499999		-0.953703	-36.972641	395.565796	41.992935
0.449999		-0.949074	-40.541343	455.692993	46.207359
0.399999		-0.944444	-44.564193	522.909547	50.918693
0.349999		-0.939814	-49.165969	599.113404	56.259956
0.299999		-0.935185	-54.530426	687.084352	62.426002
0.249999		-0.930555	-60.943855	791.131837	69.718887
0.199999		-0.925925	-68.888641	918.475831	78.644653
0.149999		-0.921296	-79.274475	1082.650882	90.151993
0.099999		-0.916666	-94.157882	1314.042971	106.370697
0.049999		-0.912036	-120.153732	1709.612308	134.096893
-0.000000		-0.907407	-559.506227	8063.708997	579.467286
	-0.899999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.995613	-15.918846	29.272075	16.318733
0.899999		-0.991228	-17.669071	60.127166	18.481426
0.849999		-0.986841	-19.529266	92.746383	20.767765
0.799999		-0.982456	-21.513210	127.343643	23.192756
0.749999		-0.978068	-23.637348	164.174560	25.774303
0.699999		-1.000000	-25.527347	203.547485	28.534023
0.649999		-0.969298	-28.390571	245.839569	31.498344
0.599999		-0.964912	-31.074569	291.518372	34.700065
0.549999		-0.960526	-34.012245	341.174134	38.180519
0.499999		-0.956140	-37.253357	395.565796	41.992935
0.449999		-0.951754	-40.863807	455.692993	46.207359
0.399999		-0.947368	-44.933158	522.909547	50.918693
0.349999		-0.942982	-49.587562	599.113404	56.259956
0.299999		-0.938596	-55.012642	687.084352	62.426002
0.249999		-0.934210	-61.497764	791.131837	69.718887
0.199999		-0.929824	-69.530349	918.475831	78.644653
0.149999		-0.925438	-80.029676	1082.650882	90.151993
0.099999		-0.921052	-95.073929	1314.042971	106.370697
0.049999		-0.916666	-121.347610	1709.612308	134.096893
-0.000000		-0.912280	-565.328980	8063.708997	579.467286

0.849999		-0.983333	-19.206710	92.746383	20.767765
0.799999		-0.977777	-21.071636	127.343643	23.192756
0.749999		-0.972221	-23.069747	164.174560	25.774303
0.699999		-1.000000	-24.960941	203.547485	28.534023
0.649999		-0.961111	-27.545681	245.839569	31.498344
0.599999		-0.955555	-30.075656	291.518372	34.700065
0.549999		-0.950000	-32.846649	341.174134	38.180519
0.499999		-0.944444	-35.905906	395.565796	41.992935
0.449999		-0.938888	-39.316009	455.692993	46.207359
0.399999		-0.933333	-43.162078	522.909547	50.918693
0.349999		-0.927777	-47.563926	599.113404	56.259956
0.299999		-0.922222	-52.697960	687.084352	62.426002
0.249999		-0.916666	-58.839004	791.131837	69.718887
0.199999		-0.911110	-66.450134	918.475831	78.644653
0.149999		-0.905555	-76.404709	1082.650882	90.151993
0.099999		-0.899999	-90.676910	1314.042971	106.370697
0.049999		-0.894444	-115.617065	1709.612308	134.096893
-0.000000		-0.888888	-537.379762	8063.708997	579.467286
	-0.600000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.994791	-15.846839	29.272075	16.318733
0.899999		-0.989583	-17.521602	60.127166	18.481426
0.849999		-0.984374	-19.302467	92.746383	20.767765
0.799999		-0.979166	-21.202724	127.343643	23.192756
0.749999		-0.973957	-23.238250	164.174560	25.774303
0.699999		-1.000000	-24.433597	203.547485	28.534023
0.649999		-0.963542	-27.796497	245.839569	31.498344
0.599999		-0.958333	-30.372211	291.518372	34.700065
0.549999		-0.953125	-33.192680	341.174134	38.180519
0.499999		-0.947916	-36.305923	395.565796	41.992935
0.449999		-0.942708	-39.775512	455.692993	46.207359
0.399999		-0.937499	-43.687858	522.909547	50.918693
0.349999		-0.932291	-48.164695	599.113404	56.259956
0.299999		-0.927083	-53.385139	687.084352	62.426002
0.249999		-0.921874	-59.628326	791.131837	69.718887
0.199999		-0.916666	-67.364578	918.475831	78.644653
0.149999		-0.911458	-77.480865	1082.650882	90.151993
0.099999		-0.906249	-91.982300	1314.042971	106.370697
0.049999		-0.901041	-117.318313	1709.612308	134.096893
-0.000000		-0.895833	-545.677247	8063.708997	579.467286
	-0.699999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.995097	-15.873664	29.272075	16.318733
0.899999		-0.990195	-17.576541	60.127166	18.481426
0.849999		-0.985293	-19.386966	92.746383	20.767765
0.799999		-0.980392	-21.318401	127.343643	23.192756
0.749999		-0.975489	-23.386936	164.174560	25.774303
0.699999		-1.000000	-24.082035	203.547485	28.534023
0.649999		-0.965686	-28.017810	245.839569	31.498344
0.599999		-0.960784	-30.633873	291.518372	34.700065
0.549999		-0.955882	-33.498008	341.174134	38.180519
0.499999		-0.950980	-36.658897	395.565796	41.992935
0.449999		-0.946078	-40.180954	455.692993	46.207359
0.399999		-0.941176	-44.151794	522.909547	50.918693
0.349999		-0.936274	-48.694770	599.113404	56.259956
0.299999		-0.931372	-53.991470	687.084352	62.426002

0.399999		-0.916666	-41.058906	522.909547	50.918693
0.349999		-0.909722	-45.160881	599.113404	56.259956
0.299999		-0.902777	-49.949264	687.084352	62.426002
0.249999		-0.895832	-55.681717	791.131837	69.718887
0.199999		-0.888888	-62.792389	918.475831	78.644653
0.149999		-0.881944	-72.100021	1082.650882	90.151993
0.099999		-0.874999	-85.455459	1314.042971	106.370697
0.049999		-0.868055	-108.812088	1709.612308	134.096893
-0.000000		-0.861110	-504.189759	8063.708997	579.467286
	-0.300000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.993589	-15.741603	29.272075	16.318733
0.899999		-0.987179	-17.306068	60.127166	18.481426
0.849999		-0.980769	-18.970996	92.746383	20.767765
0.799999		-0.974358	-20.748951	127.343643	23.192756
0.749999		-0.967948	-22.654975	164.174560	25.774803
0.699999		-1.000000	-23.613285	203.547485	28.534023
0.649999		-0.955128	-26.928257	245.839569	31.498344
0.599999		-0.948718	-29.345703	291.518372	34.700065
0.549999		-0.942307	-31.994857	341.174134	38.180519
0.499999		-0.935897	-34.921203	395.565796	41.992935
0.449999		-0.929487	-38.184913	455.692993	46.207359
0.399999		-0.923076	-41.867813	522.909547	50.918693
0.349999		-0.916666	-46.085136	599.113404	56.259956
0.299999		-0.910256	-51.006454	687.084352	62.426002
0.249999		-0.903845	-56.896064	791.131837	69.718887
0.199999		-0.897435	-64.199234	918.475831	78.644653
0.149999		-0.891025	-73.755676	1082.650882	90.151993
0.099999		-0.884615	-87.463730	1314.042971	106.370697
0.049999		-0.878204	-111.429397	1709.612308	134.096893
-0.000000		-0.871794	-516.955201	8063.708997	579.467286
	-0.400000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.994047	-15.781692	29.272075	16.318733
0.899999		-0.988095	-17.388176	60.127166	18.481426
0.849999		-0.982142	-19.097271	92.746383	20.767765
0.799999		-0.976190	-20.921817	127.343643	23.192756
0.749999		-0.970237	-22.877182	164.174560	25.774803
0.699999		-1.000000	-23.574222	203.547485	28.534023
0.649999		-0.958333	-27.259025	245.839569	31.498344
0.599999		-0.952381	-29.736751	291.518372	34.700065
0.549999		-0.946428	-32.451164	341.174134	38.180519
0.499999		-0.940476	-35.448715	395.565796	41.992935
0.449999		-0.934523	-38.790847	455.692993	46.207359
0.399999		-0.928571	-42.561157	522.909547	50.918693
0.349999		-0.922618	-46.877349	599.113404	56.259956
0.299999		-0.916666	-51.912605	687.084352	62.426002
0.249999		-0.910713	-57.936912	791.131837	69.718887
0.199999		-0.904761	-65.405059	918.475831	78.644653
0.149999		-0.898809	-75.174789	1082.650882	90.151993
0.099999		-0.892856	-89.185074	1314.042971	106.370697
0.049999		-0.886904	-113.672805	1709.612308	134.096893
-0.000000		-0.880952	-527.896729	8063.708997	579.467286
	-0.500000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.994444	-15.816436	29.272075	16.318733
0.899999		-0.988888	-17.459335	60.127166	18.481426

1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.991666	-15.573221	29.272075	16.318733
0.899999		-0.983333	-16.961219	60.127166	18.481426
0.849999		-0.975000	-18.440635	92.746383	20.767765
0.799999		-0.966666	-20.022907	127.343643	23.192756
0.749999		-0.958333	-21.721729	164.174560	25.774303
0.699999		-1.000000	-22.724613	203.547485	28.534023
0.649999		-0.941667	-25.539085	245.839569	31.498344
0.599999		-0.933333	-27.703277	291.518372	34.700065
0.549999		-0.925000	-30.078346	341.174134	38.180519
0.499999		-0.916666	-32.705650	395.565796	41.992935
0.449999		-0.908333	-35.639961	455.692993	46.207359
0.399999		-0.899999	-38.955741	522.909547	50.918693
0.349999		-0.891666	-42.757827	599.113404	56.259956
0.299999		-0.883333	-47.200561	687.084352	62.426002
0.249999		-0.874999	-52.524444	791.131837	69.718887
0.199999		-0.866666	-59.134651	918.475831	78.644653
0.149999		-0.858333	-67.795364	1082.650882	90.151993
0.099999		-0.849999	-80.234024	1314.042971	106.370697
0.049999		-0.841666	-102.007110	1709.612308	134.096893
-0.000000		-0.833332	-470.999817	8063.708997	579.467286
	-0.100000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.992424	-15.639551	29.272075	16.318733
0.899999		-0.984848	-17.097068	60.127166	18.481426
0.849999		-0.977272	-18.649559	92.746383	20.767765
0.799999		-0.969696	-20.308918	127.343643	23.192756
0.749999		-0.962120	-22.089366	164.174560	25.774303
0.699999		-1.062500	-24.580081	203.547485	28.534023
0.649999		-0.946970	-26.086330	245.839569	31.498344
0.599999		-0.939394	-28.350292	291.518372	34.700065
0.549999		-0.931818	-30.833324	341.174134	38.180519
0.499999		-0.924242	-33.578437	395.565796	41.992935
0.449999		-0.916666	-36.642509	455.692993	46.207359
0.399999		-0.909090	-40.102897	522.909547	50.918693
0.349999		-0.901514	-44.068565	599.113404	56.259956
0.299999		-0.893939	-48.699836	687.084352	62.426002
0.249999		-0.886363	-54.246589	791.131837	69.718887
0.199999		-0.878787	-61.129760	918.475831	78.644653
0.149999		-0.871211	-70.143341	1082.650882	90.151993
0.099999		-0.863636	-83.082061	1314.042971	106.370697
0.049999		-0.856060	-105.718918	1709.612308	134.096893
-0.000000		-0.848484	-489.103394	8063.708997	579.467286
	-0.200000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.993055	-15.694826	29.272075	16.318733
0.899999		-0.986111	-17.210277	60.127166	18.481426
0.849999		-0.979166	-18.823669	92.746383	20.767765
0.799999		-0.972221	-20.547267	127.343643	23.192756
0.749999		-0.965276	-22.395732	164.174560	25.774303
0.699999		-1.000000	-23.398441	203.547485	28.534023
0.649999		-0.951389	-26.542377	245.839569	31.498344
0.599999		-0.944444	-28.889469	291.518372	34.700065
0.549999		-0.937500	-31.462490	341.174134	38.180519
0.499999		-0.930555	-34.305778	395.565796	41.992935
0.449999		-0.923611	-37.477989	455.692993	46.207359

0.499999		-0.880952	-28.591045	395.565796	41.992935
0.449999		-0.869047	-30.913604	455.692993	46.207359
0.399999		-0.857142	-33.547569	522.909547	50.918693
0.349999		-0.845237	-36.578521	599.113404	56.259956
0.299999		-0.833332	-40.132454	687.084352	62.426002
0.249999		-0.821427	-44.405685	791.131837	69.718887
0.199999		-0.809523	-49.728988	918.475831	78.644653
0.149999		-0.797618	-56.726142	1082.650882	90.151993
0.099999		-0.785713	-66.807373	1314.042971	106.370697
0.049999		-0.773808	-84.508529	1709.612308	134.096893
-0.000000		-0.761904	-385.654297	8063.708997	579.467286
	0.199999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.989583	-15.390806	29.272075	16.318733
0.899999		-0.979166	-16.587627	60.127166	18.481426
0.849999		-0.968750	-17.866077	92.746383	20.767765
0.799999		-0.958333	-19.236354	127.343643	23.192756
0.749999		-0.947916	-20.710697	164.174560	25.774303
0.699999		-0.937500	-21.015628	203.547485	28.534023
0.649999		-0.927083	-24.034118	245.839569	31.498344
0.599999		-0.916666	-25.923980	291.518372	34.700065
0.549999		-0.906249	-28.002109	341.174134	38.180519
0.499999		-0.895833	-30.305469	395.565796	41.992935
0.449999		-0.885416	-32.882919	455.692993	46.207359
0.399999		-0.874999	-35.800972	522.909547	50.918693
0.349999		-0.864583	-39.153236	599.113404	56.259956
0.299999		-0.854166	-43.077484	687.084352	62.426002
0.249999		-0.843749	-47.788498	791.131837	69.718887
0.199999		-0.833332	-53.648002	918.475831	78.644653
0.149999		-0.822916	-61.338310	1082.650882	90.151993
0.099999		-0.812499	-72.401794	1314.042971	106.370697
0.049999		-0.802082	-91.799606	1709.612308	134.096893
-0.000000		-0.791666	-421.214966	8063.708997	579.467286
	0.099999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.990740	-15.492149	29.272075	16.318733
0.899999		-0.981481	-16.795177	60.127166	18.481426
0.849999		-0.972222	-18.185276	92.746383	20.767765
0.799999		-0.962962	-19.673324	127.343643	23.192756
0.749999		-0.953703	-21.272373	164.174560	25.774303
0.699999		-1.062500	-23.710941	203.547485	28.534023
0.649999		-0.935185	-24.870204	245.839569	31.498344
0.599999		-0.925926	-26.912487	291.518372	34.700065
0.549999		-0.916666	-29.155571	341.174134	38.180519
0.499999		-0.907407	-31.638900	395.565796	41.992935
0.449999		-0.898147	-34.414604	455.692993	46.207359
0.399999		-0.888888	-37.553619	522.909547	50.918693
0.349999		-0.879629	-41.155769	599.113404	56.259956
0.299999		-0.870370	-45.368087	687.084352	62.426002
0.249999		-0.861110	-50.419571	791.131837	69.718887
0.199999		-0.851851	-56.696128	918.475831	78.644653
0.149999		-0.842592	-64.925552	1082.650882	90.151993
0.099999		-0.833333	-76.753036	1314.042971	106.370697
0.049999		-0.824073	-97.470443	1709.612308	134.096893
-0.000000		-0.814814	-448.873230	8063.708997	579.467286
	-0.000000				

-0.000000		-0.583331	-172.290466	8063.708997	579.467286
	0.499999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.983333	-14.843565	29.272075	16.318733
0.899999		-0.966666	-15.466857	60.127166	18.481426
0.849999		-0.949999	-16.142395	92.746383	20.767765
0.799999		-0.933333	-16.876701	127.343643	23.192756
0.749999		-0.916665	-17.677608	164.174560	25.774303
0.699999		-0.937500	-18.720706	203.547485	28.534023
0.649999		-0.883333	-19.519268	245.839569	31.498344
0.599999		-0.866666	-20.586101	291.518372	34.700065
0.549999		-0.849999	-21.773433	341.174134	38.180519
0.499999		-0.833332	-23.104911	395.565796	41.992935
0.449999		-0.816665	-24.611808	455.692993	46.207359
0.399999		-0.799999	-26.336689	522.909547	50.918693
0.349999		-0.783332	-28.339462	599.113404	56.259956
0.299999		-0.766665	-30.708324	687.084352	62.426002
0.249999		-0.749998	-33.580696	791.131837	69.718887
0.199999		-0.733332	-37.188110	918.475831	78.644653
0.149999		-0.716665	-41.967224	1082.650882	90.151993
0.099999		-0.699999	-48.905204	1314.042971	106.378697
0.049999		-0.683332	-61.177124	1709.612308	134.096893
-0.000000		-0.666665	-271.860291	8063.708997	579.467286
	0.399999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.986111	-15.086784	29.272075	16.318733
0.899999		-0.972222	-15.964979	60.127166	18.481426
0.849999		-0.958333	-16.908470	92.746383	20.767765
0.799999		-0.944444	-17.925434	127.343643	23.192756
0.749999		-0.930554	-19.025642	164.174560	25.774303
0.699999		-1.000000	-20.957035	203.547485	28.534023
0.649999		-0.902778	-21.525878	245.839569	31.498344
0.599999		-0.888888	-22.958496	291.518372	34.700065
0.549999		-0.874999	-24.541740	341.174134	38.180519
0.499999		-0.861110	-26.305156	395.565796	41.992935
0.449999		-0.847221	-28.287860	455.692993	46.207359
0.399999		-0.833332	-30.543037	522.909547	50.918693
0.349999		-0.819443	-33.145584	599.113404	56.259956
0.299999		-0.805554	-36.205734	687.084352	62.426002
0.249999		-0.791665	-39.895279	791.131837	69.718887
0.199999		-0.777777	-44.503624	918.475831	78.644653
0.149999		-0.763888	-50.576599	1082.650882	90.151993
0.099999		-0.749999	-59.348144	1314.042971	106.378697
0.049999		-0.736110	-74.787109	1709.612308	134.096893
-0.000000		-0.722221	-338.240174	8063.708997	579.467286
	0.299999				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.988095	-15.260509	29.272075	16.318733
0.899999		-0.976190	-16.320777	60.127166	18.481426
0.849999		-0.964285	-17.455673	92.746383	20.767765
0.799999		-0.952380	-18.674530	127.343643	23.192756
0.749999		-0.940475	-19.988529	164.174560	25.774303
0.699999		-1.000000	-21.826175	203.547485	28.534023
0.649999		-0.916667	-22.959163	245.839569	31.498344
0.599999		-0.904761	-24.653060	291.518372	34.700065
0.549999		-0.892856	-26.519092	341.174134	38.180519

0.649999		-0.708331	-1.459820	245.839569	31.498344
0.599999		-0.666664	0.765420	291.518372	34.700065
0.549999		-0.624998	3.141269	341.174134	38.180519
0.499999		-0.583330	5.697510	395.565796	41.992935
0.449999		-0.541664	8.472623	455.692993	46.207359
0.399999		-0.499997	11.520416	522.909547	50.918693
0.349999		-0.458331	14.915569	599.113404	56.259956
0.299999		-0.416663	18.768344	687.084352	62.426002
0.249999		-0.374997	23.250495	791.131837	69.718887
0.199999		-0.333331	28.651443	918.475831	78.644653
0.149999		-0.291662	35.517051	1082.650882	90.151993
0.099999		-0.249997	45.081184	1314.042971	106.370697
0.049999		-0.208330	61.312774	1709.612308	134.096893
-0.000000		-0.166663	325.558411	8063.708997	579.467286
	0.700000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.833333	-11.889160	29.272075	16.318733
0.899999		-0.666666	-9.511327	60.127166	18.481426
0.849999		-0.499999	-7.133490	92.746383	20.767765
0.799999		-0.333332	-4.755655	127.343643	23.192756
0.749999		-0.166665	-2.377819	164.174560	25.774303
0.699999		0.000001	0.000017	203.547485	28.534023
0.649999		0.166668	2.377852	245.839569	31.498344
0.599999		0.333334	4.755687	291.518372	34.700065
0.549999		0.500001	7.133523	341.174134	38.180519
0.499999		0.666668	9.511358	395.565796	41.992935
0.449999		0.833335	11.889188	455.692993	46.207359
0.399999		1.000001	14.267021	522.909547	50.918693
0.349999		1.166668	16.644855	599.113404	56.259956
0.299999		1.333335	19.022686	687.084352	62.426002
0.249999		1.500001	21.400520	791.131837	69.718887
0.199999		1.666668	23.778350	918.475831	78.644653
0.149999		1.833335	26.156185	1082.650882	90.151993
0.099999		2.000001	28.534015	1314.042971	106.370697
0.049999		2.166668	30.911846	1709.612308	134.096893
-0.000000		2.333334	33.289680	8063.708997	579.467286
	0.600000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.979166	-14.478736	29.272075	16.318733
0.899999		-0.958333	-14.719678	60.127166	18.481426
0.849999		-0.937499	-14.993272	92.746383	20.767765
0.799999		-0.916666	-15.303600	127.343643	23.192756
0.749999		-0.895832	-15.655550	164.174560	25.774303
0.699999		-0.906250	-16.137699	203.547485	28.534023
0.649999		-0.854166	-16.509365	245.839569	31.498344
0.599999		-0.833332	-17.027519	291.518372	34.700065
0.549999		-0.812499	-17.620983	341.174134	38.180519
0.499999		-0.791665	-18.304538	395.565796	41.992935
0.449999		-0.770832	-19.097736	455.692993	46.207359
0.399999		-0.749999	-20.027175	522.909547	50.918693
0.349999		-0.729165	-21.130298	599.113404	56.259956
0.299999		-0.708332	-22.462215	687.084352	62.426002
0.249999		-0.687498	-24.108837	791.131837	69.718887
0.199999		-0.666665	-26.214855	918.475831	78.644653
0.149999		-0.645831	-29.053180	1082.650882	90.151993
0.099999		-0.624998	-33.240806	1314.042971	106.370697
0.049999		-0.604165	-40.762138	1709.612308	134.096893

H.R.E. 2ND ORDER DIGITAL COMPENSATION FOR T = 0.025000, ALPHA = 0.700000, AND BETA = -0.800000

GAMMA	DELTA	K	K*D	EF	E+F
	1.000000				
1.000000		0.000000	0.000000	0.000000	14.266998
0.950000		0.008333	0.729655	29.272075	16.318733
0.899999		0.016666	1.494358	60.127166	18.481426
0.849999		0.025000	2.298238	92.746383	20.767765
0.799999		0.033333	3.146200	127.343643	23.192756
0.749999		0.041666	4.044109	164.174560	25.774303
0.699999		0.062500	4.624024	203.547485	28.534023
0.649999		0.058333	6.019808	245.839569	31.498344
0.599999		0.066667	7.117176	291.518372	34.700065
0.549999		0.075000	8.304906	341.174134	38.180519
0.499999		0.083333	9.600740	395.565796	41.992935
0.449999		0.091667	11.028148	455.692993	46.207359
0.399999		0.100000	12.619039	522.909547	50.918693
0.349999		0.108333	14.418350	599.113404	56.259956
0.299999		0.116667	16.492229	687.084352	62.426002
0.249999		0.125000	18.943737	791.131837	69.718887
0.199999		0.133333	21.946525	918.475831	78.644653
0.149999		0.141667	25.828102	1082.650882	90.151993
0.099999		0.150000	31.328800	1314.042971	106.370697
0.049999		0.158334	40.829979	1709.612308	134.096893
-0.000000		0.166667	199.139618	8063.708997	579.467286
	0.900000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.916666	-9.006317	29.272075	16.318733
0.899999		-0.833332	-3.511999	60.127166	18.481426
0.849999		-0.749999	2.243513	92.746383	20.767765
0.799999		-0.666666	8.292896	127.343643	23.192756
0.749999		-0.583332	14.675275	164.174560	25.774303
0.699999		-0.250000	21.992191	203.547485	28.534023
0.649999		-0.416662	28.639263	245.839569	31.498344
0.599999		-0.333329	36.351287	291.518372	34.700065
0.549999		-0.249995	44.665786	341.174134	38.180519
0.499999		-0.166661	53.701011	395.565796	41.992935
0.449999		-0.083328	63.613342	455.692993	46.207359
0.399999		0.000005	74.615600	522.909547	50.918693
0.349999		0.083337	87.007293	599.113404	56.259956
0.299999		0.166672	101.229461	687.084352	62.426002
0.249999		0.250005	117.969162	791.131837	69.718887
0.199999		0.333337	138.384033	918.475831	78.644653
0.149999		0.416674	164.657501	1082.650882	90.151993
0.099999		0.500005	201.725159	1314.042971	106.370697
0.049999		0.583339	265.462586	1709.612308	134.096893
-0.000000		0.666673	1321.256106	8063.708997	579.467286
	0.800000				
1.000000		-1.000000	-14.266998	0.000000	14.266998
0.950000		-0.958333	-12.654598	29.272075	16.318733
0.899999		-0.916666	-10.983787	60.127166	18.481426
0.849999		-0.874999	-9.247678	92.746383	20.767765
0.799999		-0.833332	-7.438101	127.343643	23.192756
0.749999		-0.791666	-5.545279	164.174560	25.774303
0.699999		-0.687500	-3.417969	203.547485	28.534023

```
// JOB T
// FOR
*LISTALL
*IOCS(CARD,1132 PRINTER)
*NAMECOMP2
      REAL K,K1,K2
C
      READ(2,1)T,ALPHA,BETA
    1 FORMAT(3F10.0)
C
      WRITE(3,2)T,ALPHA,BETA
    2 FORMAT('1H,R.E. 2ND ORDER DIGITAL COMPENSATION FOR T = 'F10.6', AL
     1PHA =  'F10.6', AND BETA =  'F10.6//10X'GAMMA'15X'DELTA'19X'K'17X'
     2K*D'18X'EF'17X'E+F'/)
C
      DELTA=1.
C
      DO 20 I=1,20
      WRITE(3,3)DELTA
      GAMMA=1.
    3 FORMAT(15X,F20.6)
C
      DO 10 J=1,21
C
C
      K1=(ALPHA-BETA)*(GAMMA-1.)*(ALPHA-DELTA)/(ALPHA-GAMMA)/(1.-BETA)/(
     11.-DELTA)
      K2=(DELTA-GAMMA)*(K1/(ALPHA-DELTA)+1./(1.-DELTA))
C
      K=K1+K2
      CA=       (K1*ALOG(1./GAMMA)+K2*ALOG(1./ALPHA))/T
      C=ALOG(1./GAMMA)*ALOG(1./ALPHA)/T**2
      D=ALOG(1./ALPHA/GAMMA)/T
C
      WRITE(3,4)GAMMA,K,CA,C,D
    4 FORMAT(F15.6,20X,4F20.6)
C
   10 GAMMA=GAMMA-.05
C
   20 DELTA=DELTA-.1
C
      STOP
      END

VARIABLE ALLOCATIONS
 K     =0000  K1    =0002  K2    =0004  T     =0006  ALPHA=0008  BETA =000A  DELTA=000C  GAMMA=000E  CA    =0010  C     =0012
 D     =0014  I     =0020  J     =0022

STATEMENT ALLOCATIONS
 1     =0030  2     =0033  3     =007A  4     =007D  10    =0167  20    =0175

FEATURES SUPPORTED
 IOCS

CALLED SUBPROGRAMS
 FALOG   FADD    FSUB    FMPY    FDIV    FLD     FSTO    FDVR    FAXI    SRED    SWRT    SCOMP   SFIO    SIOF    STOP
 CARDZ   PRNTZ
```

H.R.E. DIGITAL COMPENSATION CALCULATIONS FOR A SAMPLING PERIOD OF 0.0250000 SECONDS

ALPHA	1/RS	VALUES OF K FOR VARYING BETA/ALPHA AND ALPHA					
BETA/ALPHA =		2	4	10	20	40	50
0.000000	0.000000	0.500000	0.750000	0.900000	0.950000	0.975000	0.980000
0.500000	0.496893	0.493827	0.740740	0.888889	0.938271	0.962963	0.967901
1.000000	0.987699	0.487804	0.731707	0.878048	0.926829	0.951219	0.956097
1.500000	1.472555	0.481927	0.722891	0.867470	0.915662	0.939759	0.944578
2.000000	1.951604	0.476190	0.714285	0.857142	0.904761	0.928571	0.933333
2.500000	2.424976	0.470588	0.705882	0.847059	0.894117	0.917647	0.922353
3.000000	2.892819	0.465116	0.697674	0.837209	0.883721	0.906976	0.911628
3.500000	3.355254	0.459770	0.689655	0.827586	0.873563	0.896551	0.901149
4.000000	3.812404	0.454545	0.681818	0.818181	0.863636	0.886363	0.890909
4.500000	4.264388	0.449438	0.674157	0.808988	0.853932	0.876404	0.880898
5.000000	4.711313	0.444444	0.666666	0.800000	0.844444	0.866666	0.871111
5.500000	5.153308	0.439560	0.659340	0.791208	0.835165	0.857142	0.861538
6.000000	5.590473	0.434782	0.652173	0.782608	0.826086	0.847826	0.852174
6.500000	6.022911	0.430107	0.645161	0.774193	0.817204	0.838709	0.843010
7.000000	6.450725	0.425531	0.638297	0.765957	0.808510	0.829787	0.834042
7.500000	6.874003	0.421052	0.631579	0.757894	0.800000	0.821052	0.825263
8.000001	7.292857	0.416666	0.625000	0.750000	0.791666	0.812500	0.816666
8.500001	7.707368	0.412371	0.618556	0.742268	0.783505	0.804123	0.808247
9.000001	8.117631	0.408163	0.612244	0.734694	0.775510	0.795918	0.800000
9.500001	8.523727	0.404040	0.606060	0.727272	0.767676	0.787878	0.791919
10.000001	8.925735	0.400000	0.600000	0.720000	0.760000	0.780000	0.784000
10.500001	9.323751	0.396039	0.594059	0.712871	0.752475	0.772277	0.776237
11.000001	9.717844	0.392156	0.588235	0.705882	0.745098	0.764705	0.768627
11.500001	10.108093	0.388349	0.582524	0.699029	0.737864	0.757281	0.761165
12.000001	10.494567	0.384615	0.576923	0.692307	0.730769	0.750000	0.753846
12.500001	10.877342	0.380952	0.571428	0.685714	0.723809	0.742857	0.746666
13.000001	11.256496	0.377358	0.566037	0.679245	0.716981	0.735849	0.739622
13.500001	11.632083	0.373831	0.560747	0.672897	0.710280	0.728972	0.732710
14.000001	12.004180	0.370370	0.555555	0.666666	0.703703	0.722222	0.725925
14.500001	12.372848	0.366972	0.550458	0.660550	0.697247	0.715596	0.719266
15.000001	12.738142	0.363636	0.545454	0.654545	0.690909	0.709091	0.712727
15.500001	13.100139	0.360360	0.540540	0.648648	0.684684	0.702702	0.706306
16.000003	13.458885	0.357142	0.535714	0.642857	0.678571	0.696428	0.700000
16.500003	13.814445	0.353982	0.530973	0.637168	0.672566	0.690265	0.693805
17.000003	14.166870	0.350877	0.526315	0.631579	0.666666	0.684210	0.687719
17.500003	14.516212	0.347826	0.521739	0.626087	0.660869	0.678260	0.681739
18.000003	14.862533	0.344827	0.517241	0.620689	0.655172	0.672413	0.675862
18.500003	15.205888	0.341880	0.512820	0.615384	0.649572	0.666666	0.670085
19.000003	15.546314	0.338983	0.508474	0.610169	0.644067	0.661016	0.664406
19.500003	15.883873	0.336134	0.504201	0.605042	0.638655	0.655462	0.658823
20.000003	16.218597	0.333333	0.500000	0.600000	0.633333	0.650000	0.653333
20.500003	16.550552	0.330578	0.495867	0.595041	0.628099	0.644628	0.647933
21.000003	16.879772	0.327868	0.491803	0.590164	0.622950	0.639344	0.642622
21.500003	17.206306	0.325203	0.487804	0.585365	0.617886	0.634146	0.637398
22.000003	17.530197	0.322580	0.483871	0.580645	0.612903	0.629032	0.632258
22.500003	17.851474	0.320000	0.480000	0.576000	0.608000	0.624000	0.627200
23.000003	18.170204	0.317460	0.476190	0.571428	0.603174	0.619047	0.622222
23.500003	18.486412	0.314960	0.472441	0.566929	0.598425	0.614173	0.617322
24.000003	18.800140	0.312500	0.468750	0.562500	0.593750	0.609375	0.612500
24.500003	19.111427	0.310077	0.465116	0.558139	0.589147	0.604651	0.607751

```
// JOB T
// FOR
*IOCS(CARD,1132 PRINTER)
*LISTALL
*NAMEAPPLE
      REAL K(6)
      DIMENSION B(6)
      READ(2,1)T,A,DA
    1 FORMAT(3F10.0)
C
      WRITE(3,2)T
    2 FORMAT('1 H.R.E. DIGITAL COMPENSATION CALCULATIONS FOR A SAMPLING
     1PERIOD OF'F10.8'   SECONDS'//68X'VALUES OF K FOR VARYING BETA/ALPH
     2A AND ALPHA'/48X'BETA/ALPHA ='7X,1H2,9X1H4,8X2H10,8X2H20,8X2H40,8X
     32H50/5X'ALPHA'5X'1/R$')
C
      B(1)=2.
      B(2)=4.
      B(3)=10.
      B(4)=20.
      B(5)=40.
      B(6)=50.
C
      DO 10 I=1,50
C
      RC=ALOG(1.+A*T)/T
C
      DO 5 J=1,6
    5 K(J)=(1.-1./B(J))/(1.+A*T)
C
      WRITE(3,3)A,RC,K
    3 FORMAT(2F15.6,30X,6F10.6)
C
   10 A=A+DA
      STOP
      END

VARIABLE ALLOCATIONS
 B    =000A  K    =0016  T    =0018  A    =001A  DA   =001C  RC   =001E  I    =0022  J    =0024

STATEMENT ALLOCATIONS
 1    =0040  2    =0043  3    =00AD  5    =0110  10   =013A

FEATURES SUPPORTED
 IOCS

CALLED SUBPROGRAMS
 FALOG   FADD    FMPY    FDIV    FDIVX   FLD     FSTO    FSTOX   FSBR    FDVR    SRED    SWRT    SCOMP   SFIO    SIOAF
 SIOF    SUBSC   STOP    CARDZ   PRNTZ

REAL CONSTANTS
  .200000E 01=002C    .400000E 01=002E    .100000E 02=0030    .200000E 02=0032    .400000E 02=0034    .500000E 02=0036
  .100000E 01=0038

INTEGER CONSTANTS
     2=003A      3=003B      1=003C     50=003D      6=003E      0=003F

CORE REQUIREMENTS FOR APPLE
```

APPENDIX D

GENERAL CHARACTERISTICS

APPENDIX D

GENERAL CHARACTERISTICS

Computer Functions

The computer performs the following functions:

- Executes 18 instructions as listed in the instruction repertoire
- Manually selects any step in a program
- Manually indexes its program one step at a time
- Automatically stops computer operation at any predetermined program step
- Provides outputs for display of memory words and storage registers
- Accepts synchronous parallel digital data under program control
- Transmits parallel digital data under program control
- Accepts serial coded digital data
- Transmits serial digital data

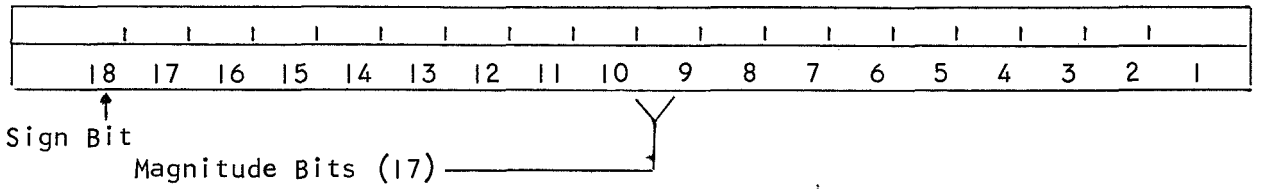
Number System

Information in the computer is organized in groups of eighteen bits called words. This word of information represents numerical data or a computer instruction. Numbers are stored in binary fixed point fractional notation. Negative numbers are represented in two's complement form.

Data Words

Data words contain one sign bit and 17 magnitude bits, as illustrated below. The most significant bit is in bit position 17, the least significant in position 1. Positive numbers have a "zero" sign bit; negative numbers, in two's complement form, have a "one" sign bit. The two's complement of a binary number is the one's complement plus one added to the least significant bit position. The only representation of zero is positive zero.

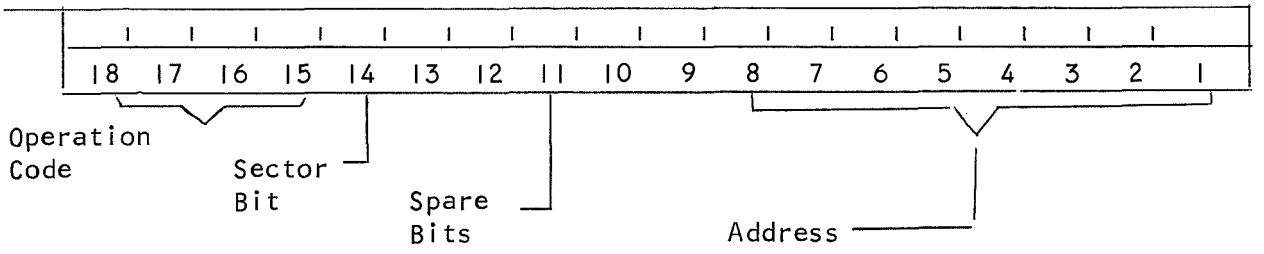
The scaling convention used assumes the binary point is between bit position S and 17 (i.e., all numbers are fractional). However, with proper scaling the binary point may be assumed to be anywhere in the number.



Computer Data Word Format

Instruction Word

The instruction word specifies the instruction to be executed and contains 4 fields as illustrated below:

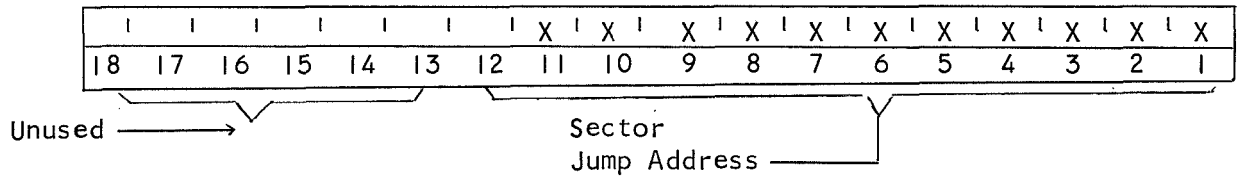


Computer Instruction Word Format

The operation code is contained in bits 15 through 18 and represents any one of the memory reference instructions available in the instruction repertoire. Bits 1 through 8 specify the address of the memory cell from which the operand is to be read.

In addition to the operation code and the address fields in the command word, there is a sector bit (Bit 14). For those instructions which reference memory, the sector bit indicates the memory sector in which the operand is located. When the sector bit is a ONE, the address portion of the instruction refers to the sector specified by the sector register. When the sector bit is ZERO, the address portion of the instruction refers to sector zero.

In the case of jump type instructions, the SECTOR BIT indicates a jump within a sector or a jump to another sector. When the sector bit is a ZERO a jump is executed within the sector. When the sector flag is a ONE, an external sector jump is performed where the jump address is contained in the memory cell addressed by the sector register and the operand address of the instruction word. The format of the memory word which contains an external transfer address is illustrated.



External Sector Jump Address Format

Instruction Repertoire

An alphabetic summary of computer instructions is presented in Figure D-1.

Instructions

1. Arithmetic Operations

For arithmetic operations, the SECTOR BIT (bit 14) has its normal effect. If it is ZERO, the address portion (Y) refers to Sector 0. If the Sector Bit is a ONE, Y refers to an address in the sector defined by the contents of the Sector Register (SR). The arithmetic operations are the following:

CLA Y $(70)_8$

Clear and Add

The contents of effective operand address in memory, bits 1 thru 18, replace the contents of the accumulator. The contents of the effective operand address in memory remain unchanged.

ADD Y $(30)_8$

Add

The contents of the effective operand address in memory are algebraically added to the contents of the accumulator. The resultant sum replaces the contents of the accumulator. The contents of the effective operand address remain unchanged. Overflow can occur.

SUB Y $(10)_8$

Subtract

The contents of the effective operand address in memory are algebraically subtracted from the contents of the accumulator. The resultant difference replaces the contents of the accumulator. The contents of the effective operand address in memory remain unchanged. Overflow can occur.

ANA Y $(50)_8$

Logical AND

The logical product of the contents of the accumulator and the contents of the effective operand address in memory is formed and the result replaces the contents of the accumulator. A ZERO is placed into the corresponding bit position in the accumulator for each ZERO in the contents of the effective operand address in memory. The contents of the corresponding bit positions in the accumulator are unchanged for each ONE in the contents of the effective operand address in memory. The contents of the effective operand address memory location are unchanged. Overflow is not possible.

Mnemonic Symbol	Octal Command Code	Word Times **	Instruction	Interrupt Capability
ADD	30	1	Add	Yes
ANA	50	1	AND to Accumulator	Yes
ALS	44	n+1	Accumulator Left Shift (n bits)	Yes after execution
ARS	40	n+1	Accumulator Right Shift (n bits)	Yes after execution
CLA	70	1	Clear and Add	Yes
DIN	00	1	Data In	Yes
DOT	34	1	Data Out	Yes
*HLT	-	1	Halt and Proceed	No
MPY	14	19	Multiply	Yes after execution
*NOP	-	1	No Operation	Yes
RJP	74	1	Return Jump	No
STA	60	1	Store Accumulator	Yes
STM	20	1	Store M Register	Yes
SUB	10	1	Subtract	Yes
TMI	24	1	Transfer on Minus Accumulator	No
TRA	64	1	Transfer	No
TZE	04	1	Transfer on Zero Accumulator	No
WOT	54	1	Word Out	Yes

* Pseudo instruction uses DOT Instruction

** 1 Word Time equals 18 microseconds

Figure D-1. Alphabetic List of Instructions

MPY Y $(14)_8$

Multiply

The contents of the accumulator are multiplied by the contents of the effective operand address in memory forming a rounded 17 bit plus sign upper product. The resultant product and sign replace the contents of the accumulator. The effective address in memory remains unchanged. Overflow is not possible with this instruction.

Store Operations

For Store instructions the SECTOR BIT (bit 9) has its normal effect.

STA Y $(60)_8$

Store Accumulator

The contents of the accumulator replace the contents of the effective operand address in memory. The contents of the accumulator are unchanged.

STM Y $(20)_8$

Store M Register

The contents of the M register replace the contents of the effective operand address in memory. The contents of the M register are replaced with the 11 bit address of the command being executed plus one.

Shift Operations

For shift operations, the SECTOR BIT is ignored.

ARSn $(40)_8$

Accumulator Right Shift

The contents of the accumulator are shifted right the number of positions specified by the least four significant bits of the instruction. The sign bit of the accumulator does not change. The sign bit is shifted into the vacant positions of the accumulator. Each bit shifted out is lost. A maximum of 31 bits shifts may be specified (bits 1 through 5 all ONE's). If a shift of 17 or more bits is specified bits 1 through 17 of the accumulator will be the same as the sign bit.

ALSn $(44)_8$

Accumulator Left Shift

The contents of the accumulator are shifted left. The number of positions specified by the least four significant bits of the instruction. A ZERO replaces the least significant bit. A maximum of 31 bit shifts may be specified (bits 1 through 5 all ONE's). If a shift of 13 or more bits is specified the contents of the accumulator will be zero.

Control Operations

As mentioned previously, in the case of transfer (or jump) instructions, the sector bit has a somewhat different significance. For TRA, TMI, and TZE instructions, a ZERO sector bit causes a jump within the sector containing the jump instruction to the operand address of the jump instruction. A ONE sector bit causes an external jump, i.e., outside the sector containing the jump instruction. For an external jump, the jump address is obtained from the 12 least significant bits of the memory cell addressed by the operand address of the jump instruction and the contents of the sector register.

For a RJP instruction, the jump address is obtained from the 12 least significant bits of the memory cell addressed by the operand address. If the SECTOR BIT is a ZERO the address portion (Y) refers to sector 0. If the SECTOR BIT is ONE, Y refers to an address in the sector defined by the contents of the sector register.

The following jump instructions are possible:

TRA Y $(64)_8$

Unconditional Transfer

If the sector bit is ZERO, the 8 bits of Y replace the least significant 8 bits of the program counter (L). The next instruction will then be executed from address Y of the sector containing the TRA instruction.

If the sector bit is ONE, the least significant 11 bits of the effective memory cell addressed by Y replace the contents of the program counter (L). The next instruction will then be executed from the address stored in the effective operand address of the TRA instruction.

The contents of the accumulator are unchanged.

TMI Y $(24)_8$

Transfer on Minus Accumulator

If the sign bit of the accumulator is ONE (i.e., negative accumulator) and the sector bit is ZERO, the 8 bits of Y replace the least significant 8 bits of the program counter (L). The next instruction will then be executed from address Y of the sector containing the TMI instruction.

If the sign bit of the accumulator is ONE and the sector bit is ONE the least significant 11 bits of the effective memory cell addressed by Y replace the contents of the program counter (L). The next instruction will then be executed from the address stored in the effective operand address of the TMI instruction.

If the sign bit of the accumulator is ZERO (positive accumulator), the computer proceeds to the next instruction in sequence.

The contents of the accumulator remain unchanged. The magnitude bits of the accumulator are not examined.

TZE Y $(04)_8$

Transfer on Zero Accumulator

If the contents of the accumulator are ZERO and the sector bit is ZERO, the 8 bits of Y replace the least significant bits of the program counter (L). The next instruction will then be executed from address Y of the sector containing the TZE instruction.

If the contents of the accumulator are ZERO and the sector bit is ONE, the least significant 11 bits of the memory cell addressed by Y replace the contents of the program counter (L). The next instruction will then be executed from the address stored in the effective operand address of the TZE instruction.

If the contents of the accumulator are not ZERO, the computer proceeds to the next instruction in sequence.

The contents of the accumulator remain unchanged.

RJP Y $(74)_8$

Return Jump

If the sector bit is ZERO, the least significant 12 bits of the memory cell addressed by Y in sector 0 replace the contents of the program counter.

If the SECTOR BIT is a ONE, the least significant 12 bits of memory cell addressed by Y in the sector defined by the contents of the sector register replace the contents of the program counter.

The contents of the accumulator remain unchanged.

HLT (Pseudo Instruction using DOT)

Halt and Proceed

The computer stops its operation and enters an idle mode. When a restart signal is received, the computer takes its next instruction from L + 1 and proceeds from there. This instruction can be used only during nonoperational, i.e., test conditions.

NOP (Pseudo Instruction using DOT)

No Operation

The computer performs no operation for one word time then takes its next instruction from L + 1 and proceeds from there.

Input/Output

Two instructions provide the input/output interface for the Arma computer. A general description of these instructions is presented below.

DIN Y $(00)_8$

DATA IN

In the input instruction the SECTOR BIT does not effect sector addressing. The SECTOR BIT enables the computer to distinguish between accepting parallel input data or serial input data.

When the SECTOR BIT is a ZERO the computer will replace the contents of Y where Y is an address in Sector 0 with the status of 18 parallel input data lines. The contents of the accumulator remain unchanged.

When the SECTOR BIT is a ONE the computer will replace the contents of the accumulator with the status of the input lines addressed by Y. Y limits the number of inputs to 256 (28) input lines.

DOT Y $(34)_8$

DATA OUT

In the Data Out instruction, the SECTOR BIT (bit 14) has its normal effect. When the SECTOR BIT is a ZERO the address portion of the instruction work refers to Sector 0. When the SECTOR BIT is a ONE the address portion refers to memory sector currently addressed by the sector register.

The contents of the effective operand address in memory is transferred to the MOR and decoded to generate required pseudo instructions, miscellaneous output controls and address data.

The contents of the accumulator remain unchanged.

WOT Y $(54)_8$

WORD OUT

In the Word Out output instruction, the SECTOR BIT (bit 14) has its normal effect. When the SECTOR BIT is a ZERO the address portion of the instruction word refers to Sector 0. When the SECTOR BIT is a ONE the address portion refers to memory sector currently addressed by the sector register.

In this instruction the contents of effective operand address in memory is transferred to the memory output register (MOR) and the data is made available external to the computer. This instruction enables the computer to transfer 18 bits of parallel digital data external to the computer.

The contents of the accumulator remain unchanged.

PROCESSOR OPERATION

The instruction flow and data flow are shown in Figures D-2 and D-3 respectively. The various computer registers and their functions are as follows:

Accumulator (AC)

This is an 18-bit register with the following functions:

- Addition and subtraction take place in the AC.
- Information to be stored in a storage cell are placed first in the AC.
- In a multiplication operation, the multiplier is in the AC at word time 1, and the seventeen most significant bits of the product plus the sign is stored in the AC at word time 19 of the cycle.
- Input discretes and BCD information are received into the computer via the accumulator.
- The logical "AND Accumulator" instruction forms in the AC with the logical "AND" product of the original contents of the accumulator and the contents of a storage cell.
- The contents of AC can be shifted left or right.
- The accumulator is not reset dynamically when power is turned on.

Sector Register (SR)

This is a 4-bit register which specifies the sector of the operand being addressed. This register can be set from $(0)_8$ to $(7)_8$ via a DOT instruction. This register is not dynamically reset when power is turned on.

Multiplier Register (M)

This 18-bit register serves a dual function. During the multiplication process, it contains the multiplier. Each word time the contents of M are shifted one place to allow examination of each multiplier bit starting with the least significant. It also is used to hold a number equal to 1 more than the address of the instruction being executed except during the first computer word time after power is turned on. An STM command will cause the contents of M to be stored in a working storage cell. This register therefore provides a linkage between a main program and a subroutine. This register is not dynamically reset when power is turned on.

Memory Output Register (MOR)

This is an 18-bit register which also serves a dual function. It is used in the transmission of data to or from memory. It is also utilized in the execution of DOT instructions. Its contents are set by a DOT instruction and are then decoded to provide various internal functions, outputs, etc. This register is dynamically reset when power is turned on.

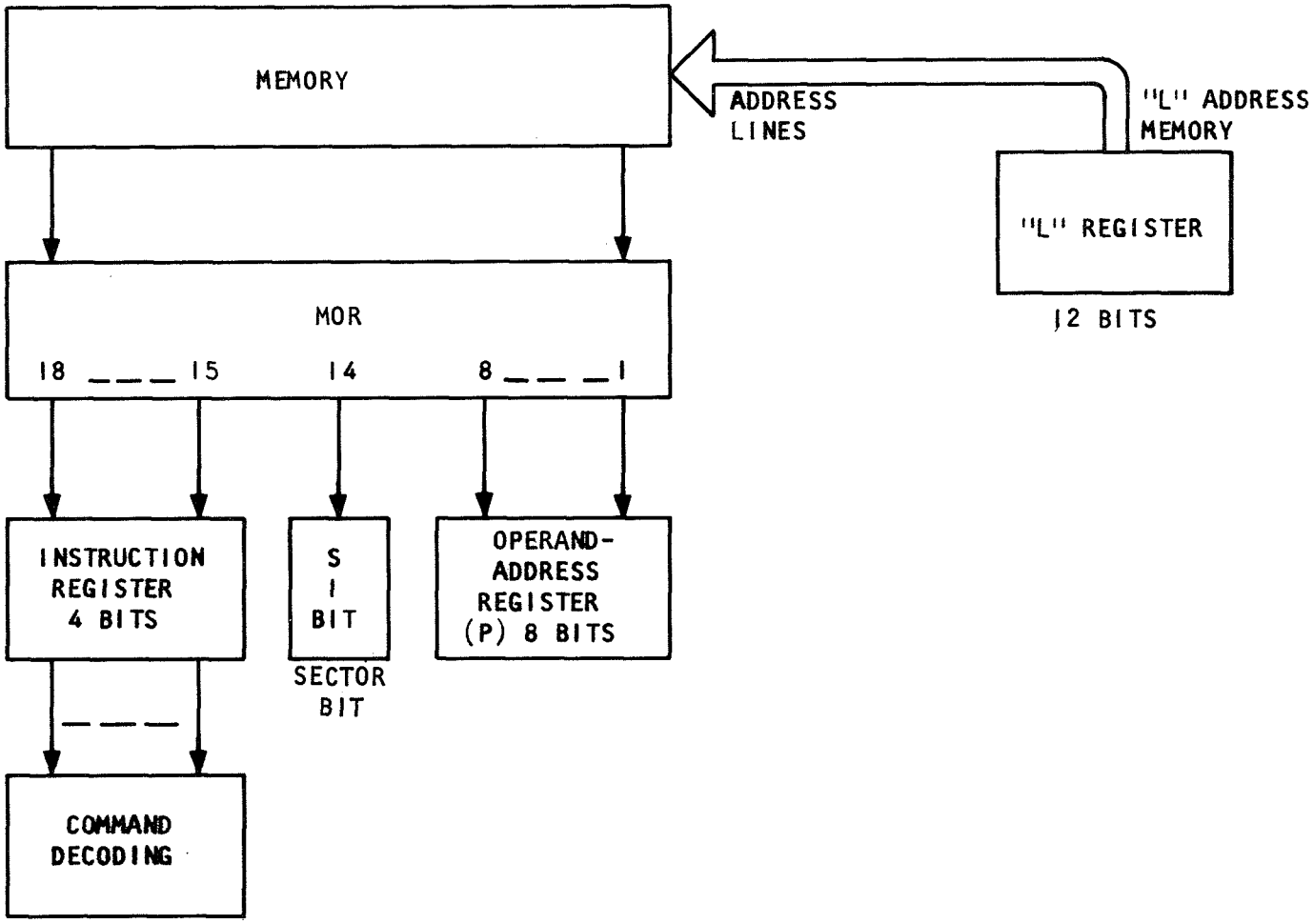


Figure D-2. Instruction Flow Diagram

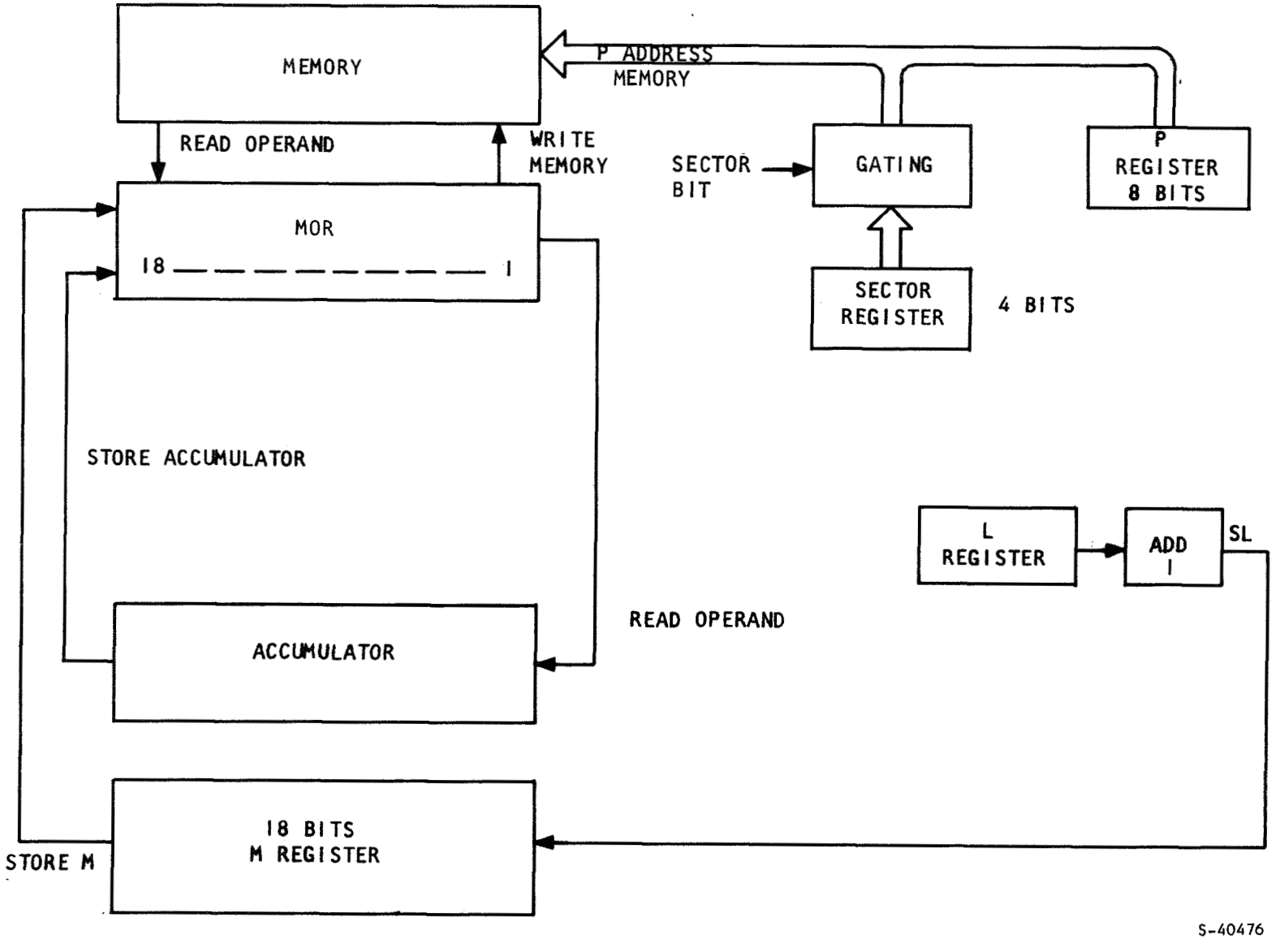


Figure D-3. Data Flow Diagram

Program Counter (L)

This is a 12-bit register which contains the address of the next instruction to be executed. The contents of the L register are incremented by one each time an instruction is executed. A branch instruction causes the transfer address to replace the contents of the L register. This register is dynamically reset to $(0400)_8$ when power is turned on.

Instruction Register (I)

This is a 4-bit register which contains the command code of the instruction being executed. This register is dynamically reset when power is turned on.

Operand Address Register (P)

This is an 8-bit register which contains the address field of the instruction being executed. During right shift it is used as a counter. This register is dynamically reset when power is turned on.

Sector Bit Register (S)

This is a one-bit register which holds the sector flag bit to determine whether an operand address refers to scratchpad or a program storage sector as specified by the contents of the Sector Register (SR). The S register is dynamically reset when power is turned on.

Memory Organization

The memory system block diagram shown in Figure D-4 is a major component breakdown of the four functional sections. Each section is covered in the following paragraphs.

Memory Stack

Computer information (both data and instructions) is retained in the memory stack which is composed of single-hole ferrite cores. The total computer memory consists of 4096 words of 18 bits. It contains 72,936 single hole ferrite cores and employs conventional coincident current memory techniques for read and store operations. All storage is non-volatile and information is not lost when power is shut off and then reapplied.

Timing and Control Section

The timing and control section provides intramemory timing and control for all of the memory logic sections. It contains the timing flip-flops and control gates required to generate the required timing pulses and is contained on two printed circuit cards. The processor presents the memory cycle commands to the timing and control section and the memory responds to the control pulses generated by these commands. Two modes of operation are available: Clear-White and Read-Restore.

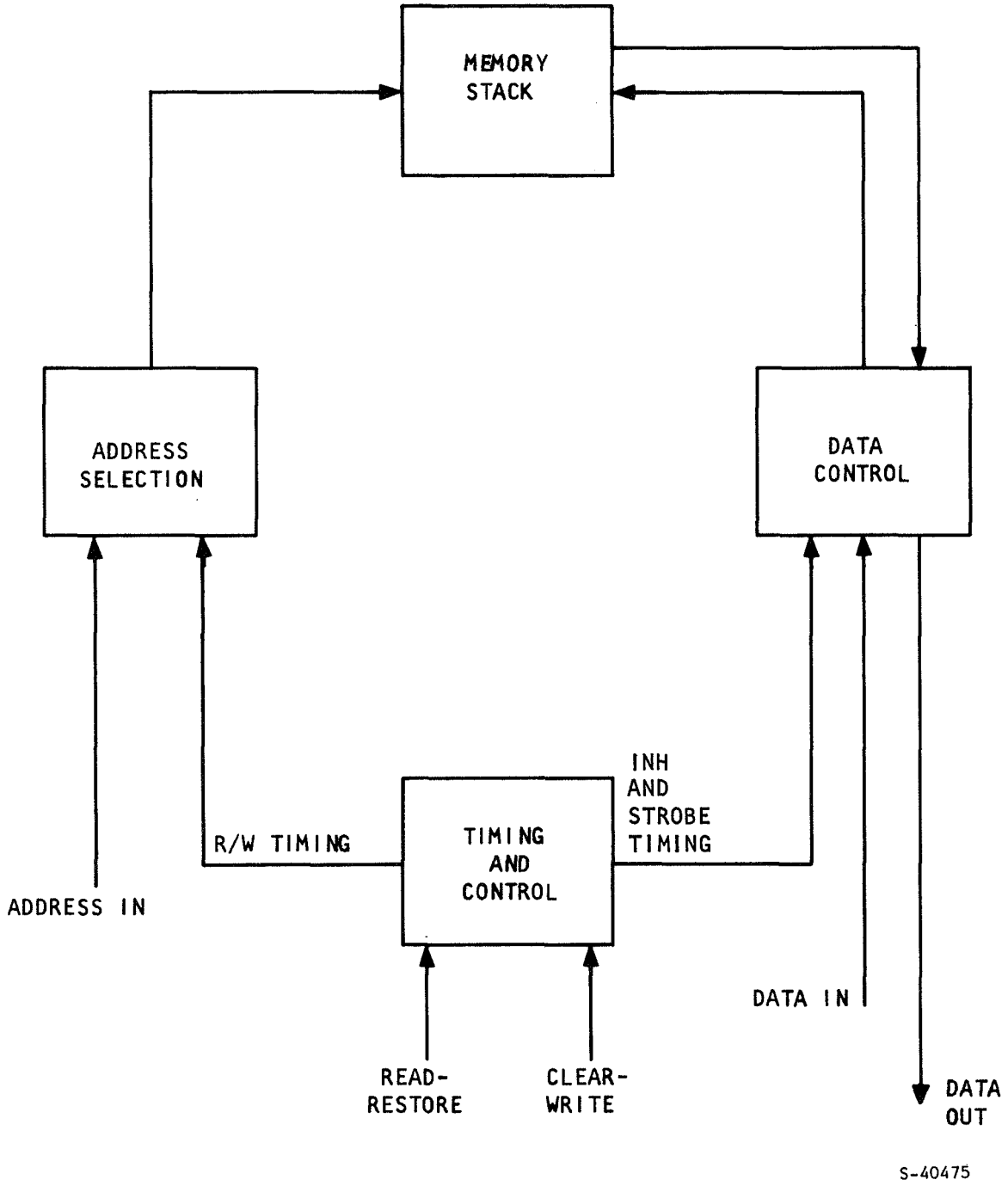


Figure D-4. Memory System Block Diagram

Address Selection

Address selection section contains the electronic components required to select any random address. The current drivers and selectors combine to provide the required drive current necessary for a read or write operation. The binary coded address inputs are presented to the memory from an external address register. These inputs are then divided into true and false components to accommodate multiple address decoding.

The memory unit is divided into 16 sectors of 256 words each. The sectors are numbered 0 through 15. Figure D-5 illustrates the assignment of memory addresses.

Data Control

The data control section provides the electronics necessary to control the loading and unloading process of the memory system. During each cycle, data is loaded into the memory by way of inhibit drivers or unloaded from the memory by way of the sense amplifiers. The processing equipment establishes the type of memory cycle to be performed and presents all of the required inputs.

Sector	12	11	10	9	8	7	6	5	4	3	2	1	Octal Representation
0	0	0	0	0	X	X	X	X	X	X	X	X	0000-0377
1	0	0	0	1	X	X	X	X	X	X	X	X	0400-0777
2	0	0	1	0	X	X	X	X	X	X	X	X	1000-1377
3	0	0	1	1	X	X	X	X	X	X	X	X	1400-1777
4	0	1	0	0	X	X	X	X	X	X	X	X	2000-2377
5	0	1	0	1	X	X	X	X	X	X	X	X	2400-2777
6	0	1	1	0	X	X	X	X	X	X	X	X	3000-3377
7	0	1	1	1	X	X	X	X	X	X	X	X	3400-3777
8	1	0	0	0	X	X	X	X	X	X	X	X	4000-4377
9	1	0	0	1	X	X	X	X	X	X	X	X	4400-4777
10	1	0	1	0	X	X	X	X	X	X	X	X	5000-5377
11	0	0	1	1	X	X	X	X	X	X	X	X	5400-5777
12	0	1	0	0	X	X	X	X	X	X	X	X	6000-6377
13	0	1	0	1	X	X	X	X	X	X	X	X	6400-6777
14	0	1	1	0	X	X	X	X	X	X	X	X	7000-7377
15	0	1	1	1	X	X	X	X	X	X	X	X	7400-7777

Figure D-5. Address Bit Configuration

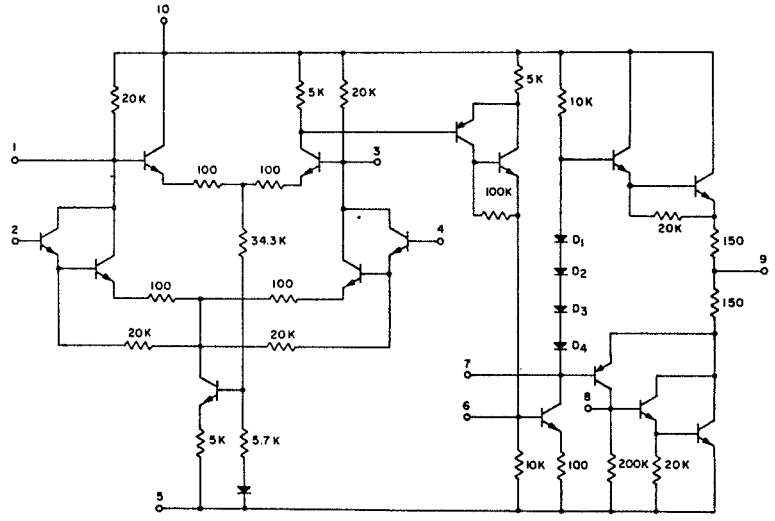
APPENDIX E

INTEGRATED CIRCUIT DATA SHEETS

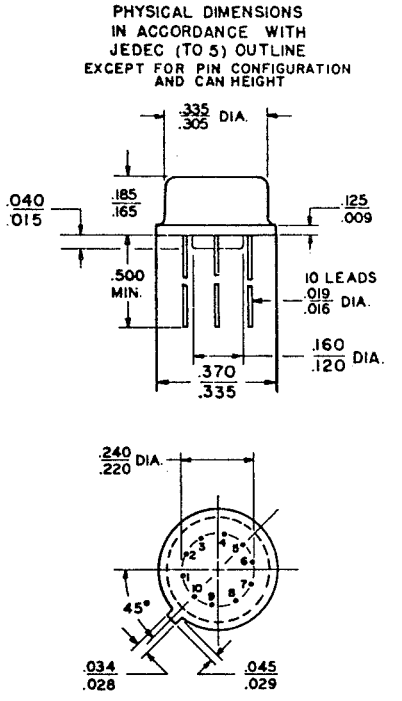
INTEGRATED CIRCUIT DATA SHEETS

AMELCO INTEGRATED OPERATIONAL AMPLIFIER 807BE

The Amelco 807BE operational amplifier is designed for ultra-high performance applications and features silicon planar construction on a single monolithic substrate. Outstanding electrical characteristics include low offset voltage and current, high input impedance, high common mode input range, excellent thermal stability and output short-circuit protection.



E Package
(TO-5)



PIN 5 IS INTERNALLY CONNECTED TO CASE
NOTE: ALL DIMENSIONS IN INCHES

TEMPERATURE RANGE:

	807BE
Temperature Range (storage)	−65°C to +150°C
Temperature Range (operating)	−55°C to +125°C
Maximum Supply Voltages	±18 V
Maximum Operating Voltages	±15 V

POWER SUPPLY REQUIREMENT:	Typ	Max
V_{CC}=±15 V	6 ma	7.5 ma

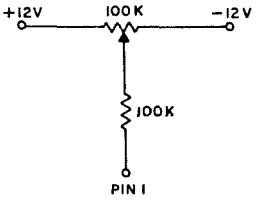
Complete part number designation consists of three digits and two letters, for example:

807 BE
- BE — Package
- BE — Temperature Range
- 807 — Circuit

ELECTRICAL CHARACTERISTICS at 25°C (Unless Otherwise Specified)

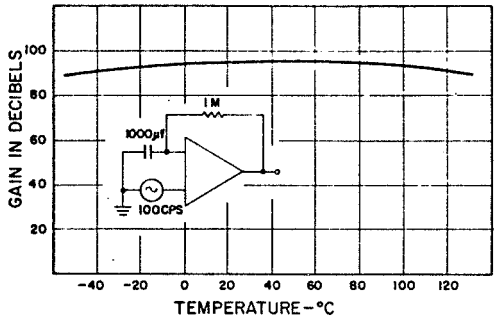
	Min.	Typ.	Max.	Units
Open Loop Voltage Gain	25,000	60,000		V/V
Input Offset Voltage		1	2.5	mV
Input Offset Voltage (−55°C to +125°C)		1.5	3.0	mV
Input Offset Voltage Drift		3	10	μV/°C
Input Offset Voltage Drift[1]		2	5	μV/°C
Input Bias Current		250	500	nA
Input Offset Current		30	50	nA
Input Offset Current Drift		.5		nA/°C
Input Impedance	500	1000		KΩ
Common Mode Range (V_{CC}=±15 V)	±7	±8		V
Common Mode Rejection Ratio		−90	−80	db
Power Supply Rejection Ratio		−80	−70	db
Output Impedance		150	300	Ω
Output Voltage Swing (V_{CC}=±15 V) (No Load)	24	26		V_{PP}
Output Voltage Swing (V_{CC}=±15 V) (1K Load)	20	24		V_{PP}

NOTE (1) With Input Offset Voltage adjusted to zero at +25°C.

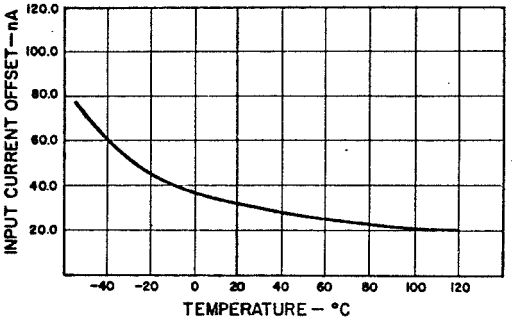


RECOMMENDED OFFSET ADJUSTMENT

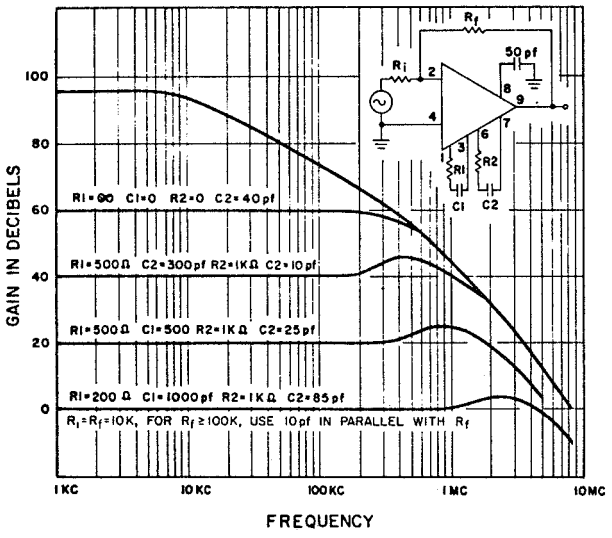
Open Loop Gain vs Temperature



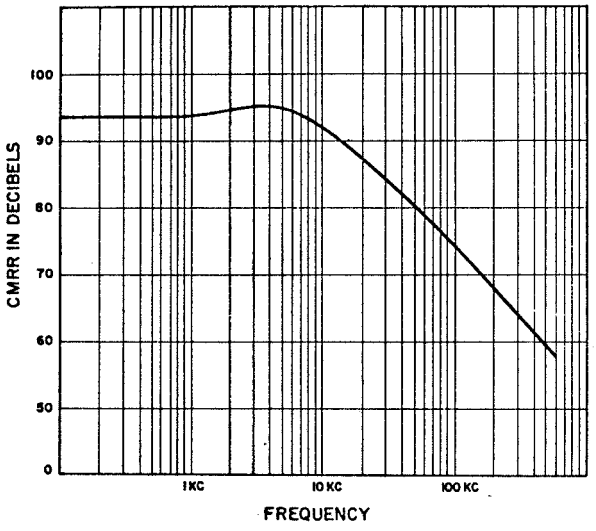
Input Offset Current vs Temperature



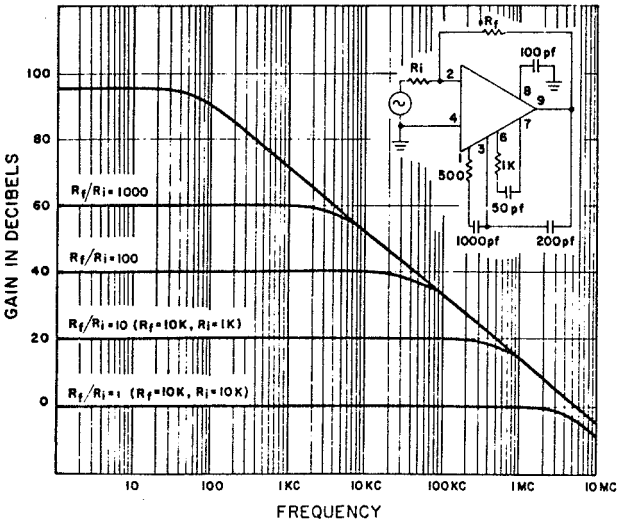
Gain vs Frequency



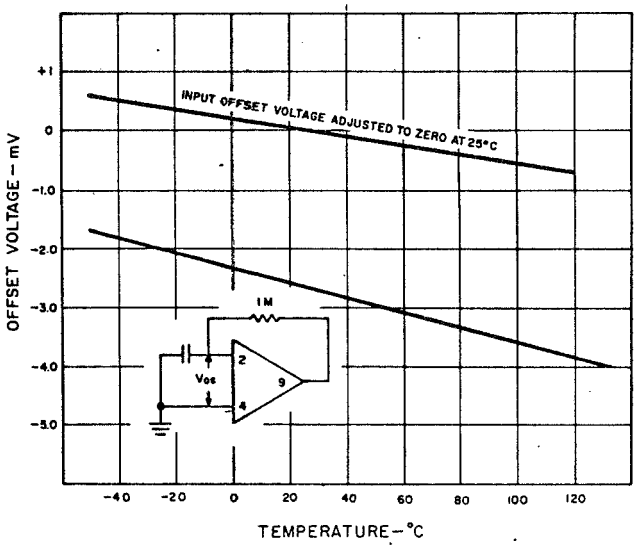
Common Mode Rejection Ratio vs Frequency



Frequency Response



Temperature vs Offset Voltage



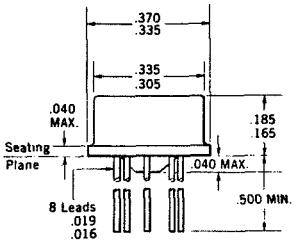
GENERAL DESCRIPTIONS - The μA709C is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For full temperature range (-55°C to +125°C) see μA709 data sheet.

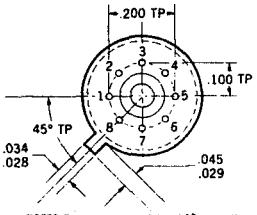
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		± 18 V
Internal Power Dissipation	(Note 1)	250 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range		-65°C to + 150°C
Operating Temperature Range		0°C to +70°C
Lead Temperature (Soldering, 60 sec)		300°C

PHYSICAL DIMENSIONS

in accordance with JEDEC(TO-99) outline

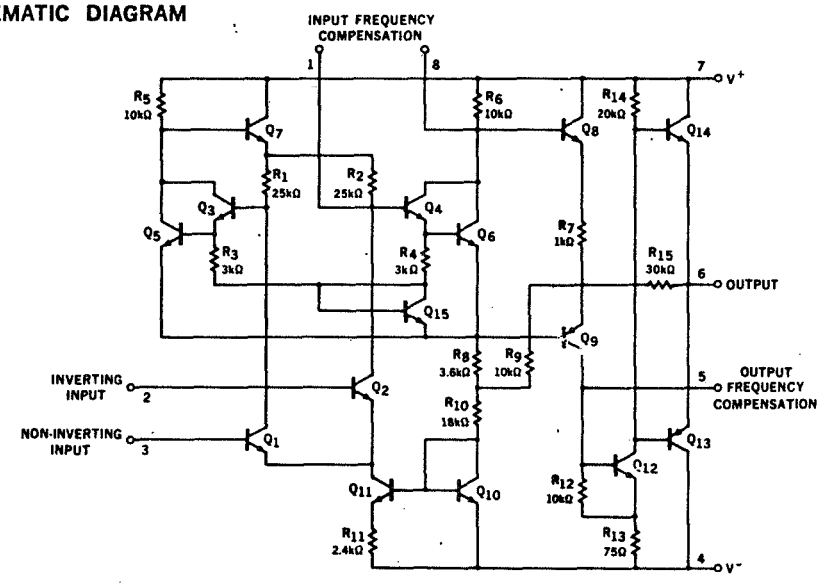




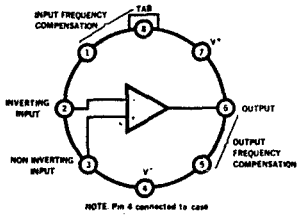
NOTES. Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.22 grams

ORDER PART NO.
U5B770939X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(Top View)

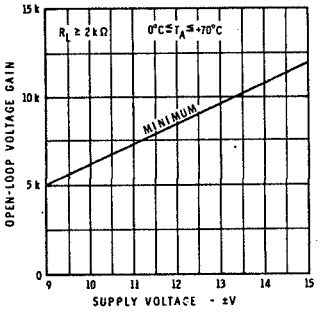
NOTE 1: Rating applies for ambient temperatures to +70°C.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

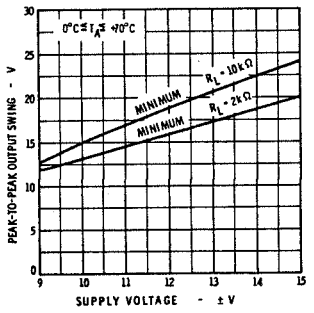
Parameter	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$, ±9 V $\leq V_S \leq$ ±15 V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, V_{out} = ±10 V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	±12	±14		V
	$R_L \geq 2\,k\Omega$	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	V_{in} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50 Ω		0.3	1.0	μs
Overshoot	$C_L \leq 100$ pF		10	30	%
The following specifications apply for 0°C $\leq T_A \leq$ +70°C					
Input Offset Voltage	$R_S \leq 10k\Omega$, ±9 V $\leq$ ±15 V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10 V	12,000			
Input Resistance		35			kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

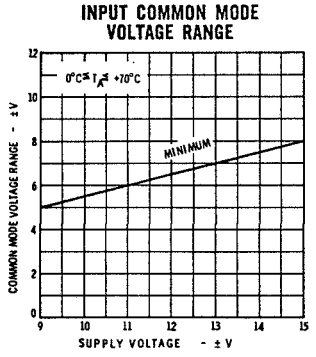
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

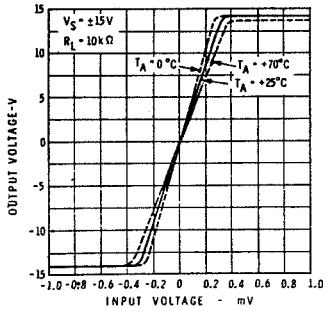


INPUT COMMON MODE VOLTAGE RANGE

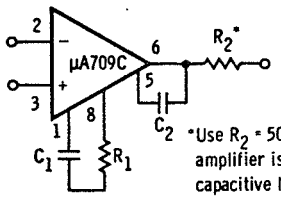


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

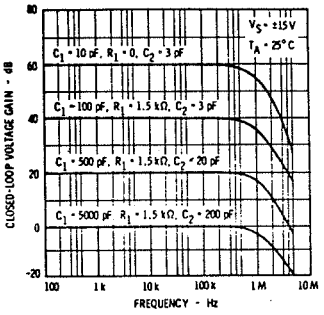


FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



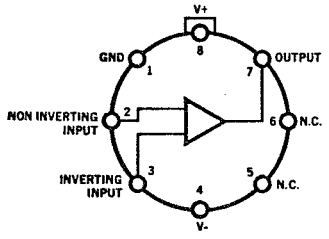
- IMPROVED SPECIFICATIONS
- 2 mV MAXIMUM OFFSET VOLTAGE
- 3 μA MAXIMUM OFFSET CURRENT
- 1250 MINIMUM VOLTAGE GAIN
- 10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT

GENERAL DESCRIPTION — The μA710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

ABSOLUTE MAXIMUM RATINGS

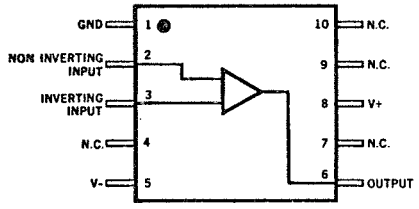
Positive Supply Voltage		+14.0 V
Negative Supply Voltage		−7.0 V
Peak Output Current		10 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Internal Power Dissipation		
TO-99	[Note 1]	300 mW
Flat Package	[Note 2]	200 mW
Operating Temperature Range		−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

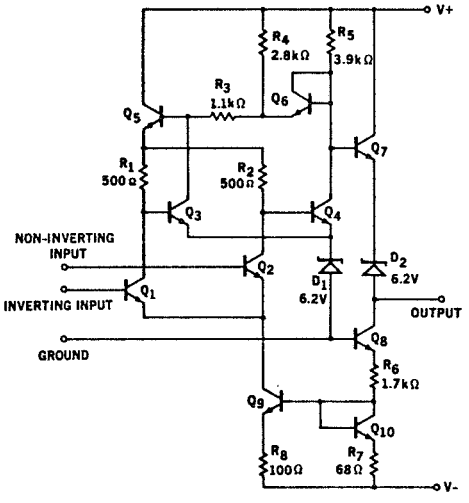


Note: Pin 4 connected to case.

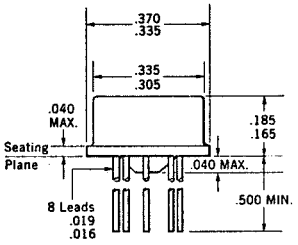
FLAT PACKAGE CONNECTION DIAGRAM
(TOP VIEW)

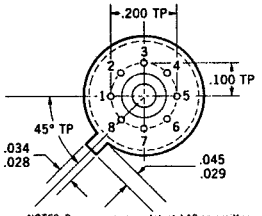


SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with JEDEC(TO-99) outline

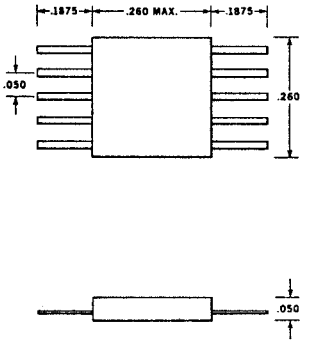




NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO.
U5B771031X

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



ORDER PART NO.
U3H771031X

Notes on page 2

* Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $V^- = 12.0V$, $V^+ = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 4)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	2.0	2.5		mA
Response Time [Note 3]			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = +125°C$ $R_S = 50\Omega$, $T_A = 25°C$ to $T_A = -55°C$		3.5 2.7	10 10	μV/°C μV/°C
Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$ $T_A = 25°C$ to $T_A = -55°C$		5.0 15	25 75	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

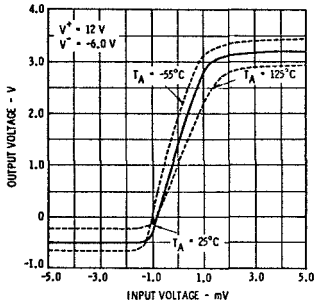
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

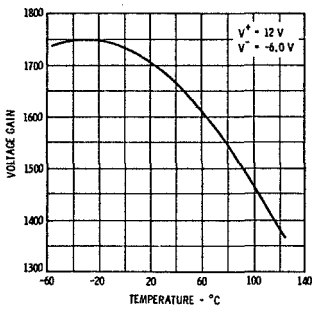
(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

TYPICAL PERFORMANCE CURVES

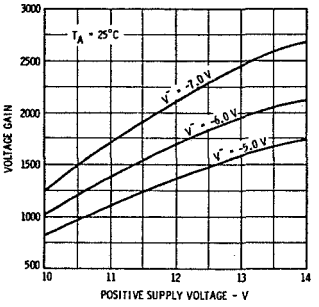
VOLTAGE TRANSFER CHARACTERISTIC



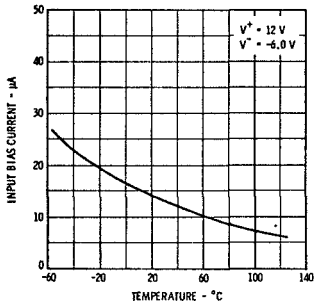
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



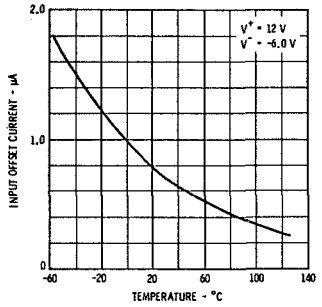
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



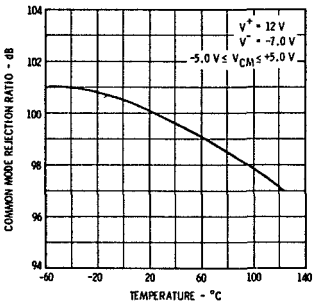
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



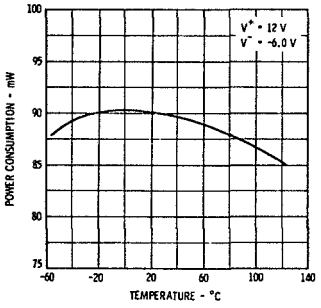
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



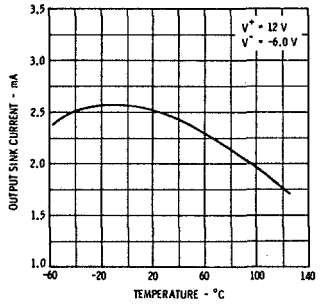
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



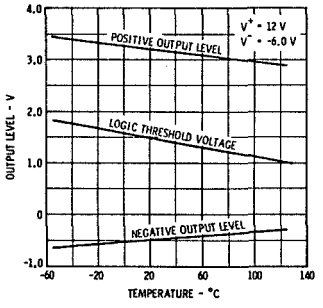
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



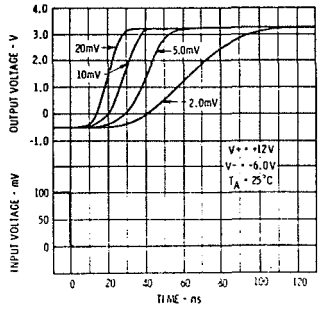
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



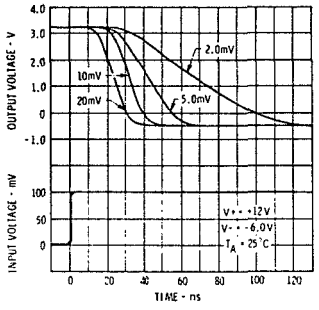
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



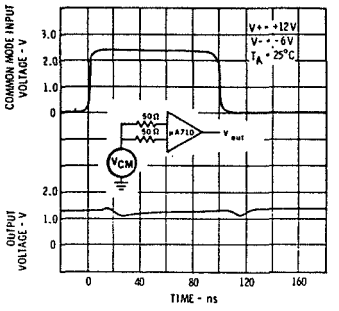
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



GENERAL DESCRIPTION — The μA726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar * process.

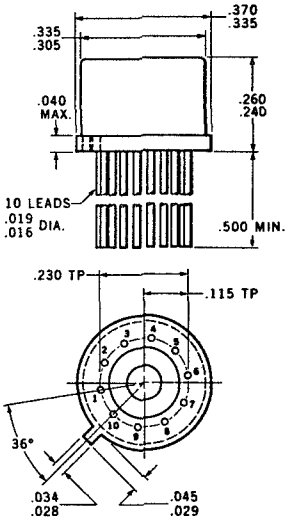
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	300°C
Supply Voltage	±18 V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

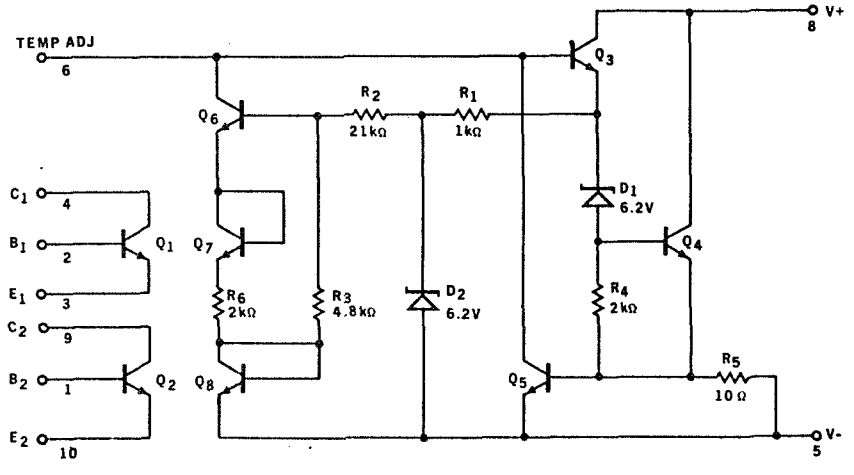
PHYSICAL DIMENSIONS



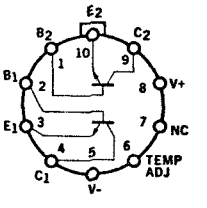
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5J772631X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

Note 1: Measured at 1 mA collector current.

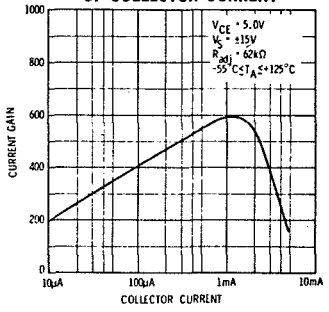
* Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)

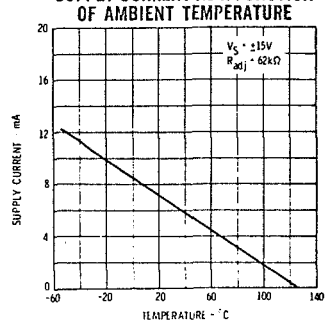
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\ \mu A \leq I_C \leq 100\ \mu A$ $V_{CE} = 5$ V, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10	50	nA
Input Offset Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		50	200	nA
Average Input Bias Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		50	150	nA
Average Input Bias Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		250	500	nA
Offset Voltage Change	$I_C = 10\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 100$ kΩ		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 10$ kΩ		0.3	6.0	mV
Input Offset Voltage Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	μV/°C
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	μV/°C
Input Offset Current Drift	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10		pA/°C
Input Offset Current Drift	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		30		pA/°C
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\ \mu A$, $R_S \leq 50\Omega$,		25		μV/V
Low-Frequency Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10 kHz		10		μV pp
Long-term Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	$f = 20$ MHz, $I_C = 100\ \mu A$, $V_{CE} = 5$ V	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5$ V		1.0		pF
Emitter Transition Capacitance	$I_E = 100\ \mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\ \mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

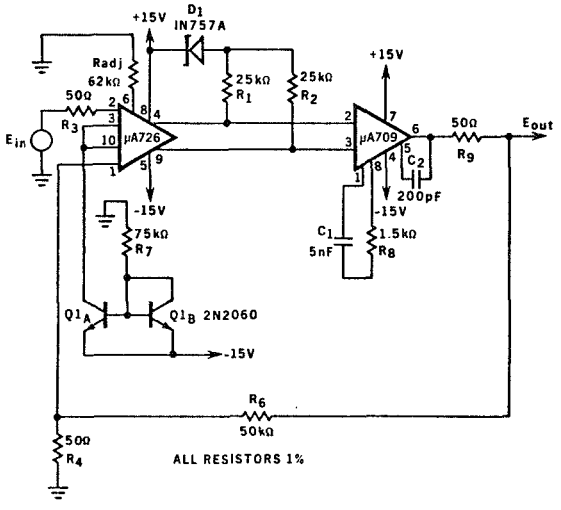
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



LM 101
operational amplifier

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Power Dissipation (Note 1) ..... 500 mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C

Electrical Characteristics (Note 4)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		40	200	nA
Input Bias Current	$T_A = 25°C$		120	500	nA
Input Resistance	$T_A = 25°C$	300	800		kΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		V/mV
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		3.0		µV/°C
	$R_S \leq 10k\Omega$		6.0		µV/°C
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		100	500	nA
Input Bias Current	$T_A = -55°C$		0.28	1.5	µA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		V
	$R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 45°C/W junction to case or 150°C/W junction to ambient (see curve).

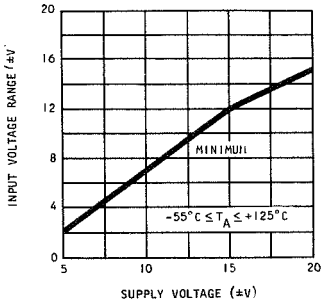
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C.

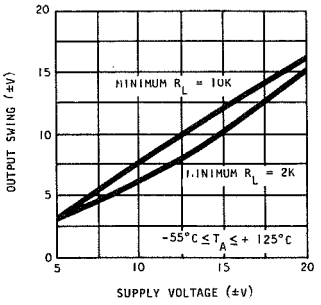
Note 4: These specifications apply for $-55°C \leq T_A \leq +125°C$, $\pm 5V \leq V_S \leq \pm 20V$ and C1 = 30 pF unless otherwise specified.

GUARANTEED PERFORMANCE

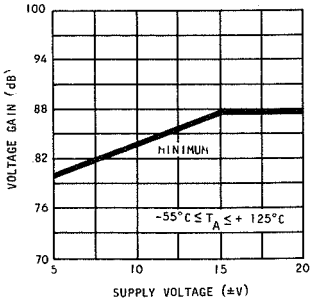
Input Voltage Range



Output Swing

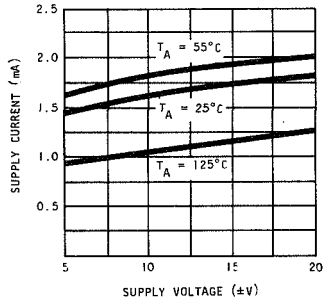


Voltage Gain

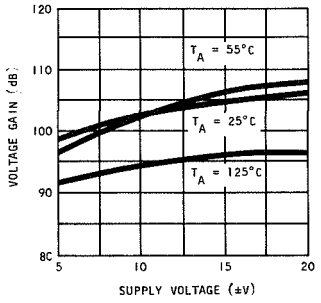


TYPICAL PERFORMANCE

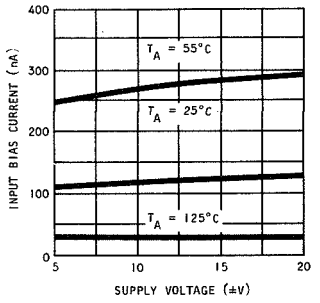
Supply Current



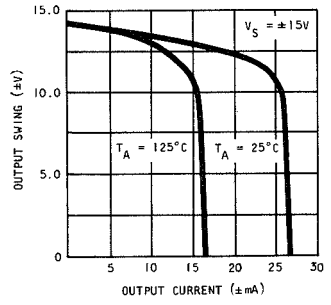
Voltage Gain



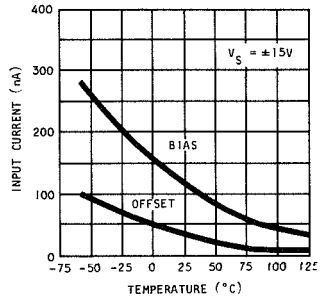
Input Bias Current



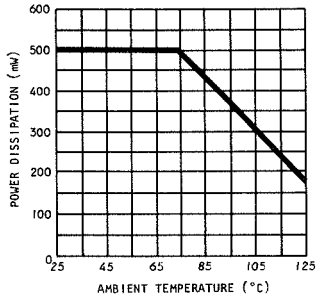
Current Limiting



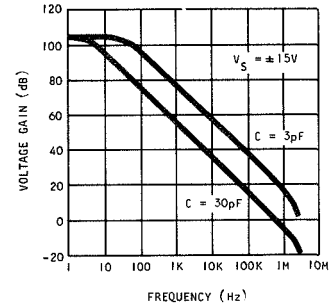
Input Current



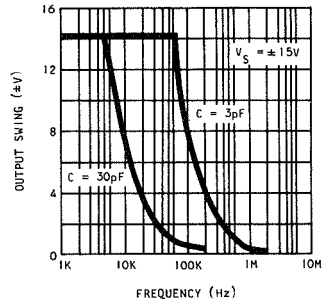
Maximum Power Dissipation



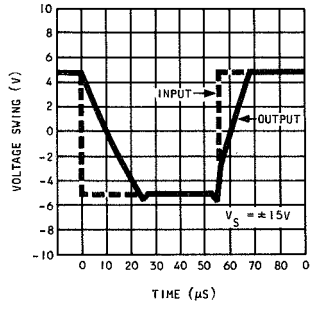
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



S-40474

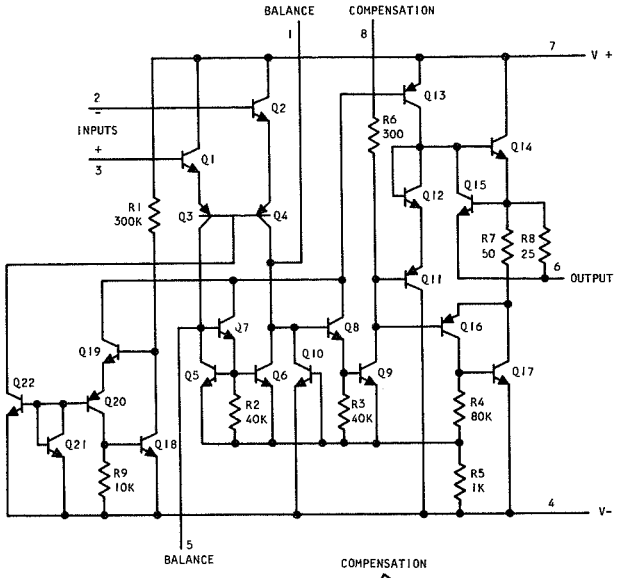
General Description

The LM101 is a general-purpose operational amplifier built on a single silicon chip. The resulting close match and tight thermal coupling gives low offsets and temperature drift as well as fast recovery from thermal transients. In addition, the device features:

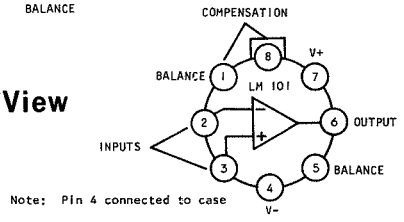
- Frequency compensation with a single 30 pF capacitor
- Operation from ±5V to ±20V
- Low current drain 1.8 mA at ±20V
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as ±30V
- No latch-up when common mode range is exceeded
- Same pin configuration as the LM709.

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. However, it is possible to optimize compensation for best high frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits. Further, the low power dissipation permits high-voltage operation and simplifies packaging in full-temperature-range systems.

Schematic and Connection Diagrams



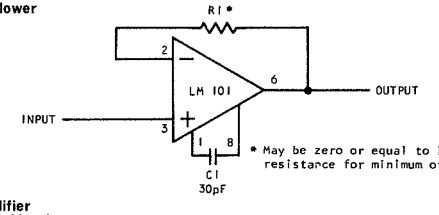
Top View



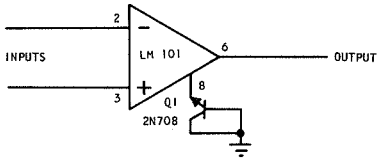
Note: Pin 4 connected to case

Typical Applications

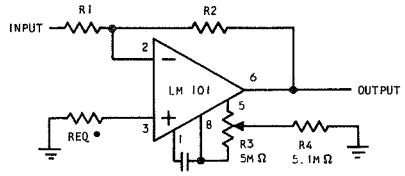
Voltage Follower



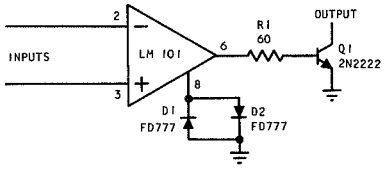
Voltage Comparator for Driving DTL or TTL Integrated Circuits



Inverting Amplifier with Balancing Circuit



Voltage Comparator for Driving RTL Logic or High Current Driver



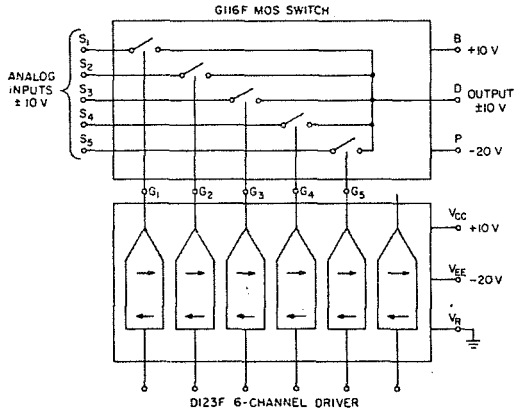
S-40473

APPLICATION

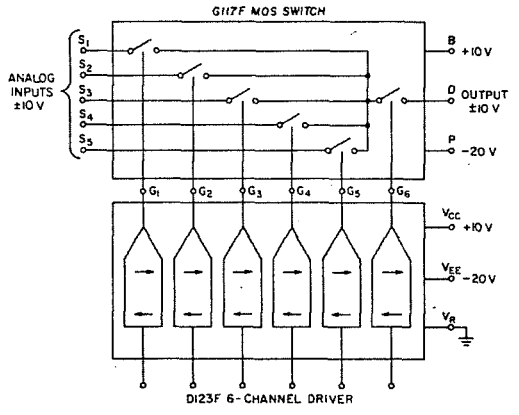
The G116F series of multiple switches, as described on page 1, is diagrammed below. The appropriate electrical bias for the single switch block shown on page 2, follows:

S Source. Analog signal input.
D Drain. Gated analog signal output.
G Control gate. Input to this terminal determines ON-OFF condition of the FET switch. To turn the switch ON, V_G should be at least 10 volts below the most negative analog signal voltage. For the OFF condition, V_G is normally equal to the body potential V_B. Supply voltages, V_{CC} and V_{EE}, for the buffer/driver circuit will determine the switching voltage levels.
B Body. Biased to the maximum positive signal voltage plus, perhaps, as much as 2 volts. The 2-volt bias will serve to reduce source-body and drain-body capacitance when the signal is at its maximum positive value.
P Pull-up gate. Biased to negative V_{EE} (negative reference for control gate waveform). This bias ensures that all pull-up FETs are turned ON, thus providing a current-limited or constant-current load for the output collector of the buffer/driver circuit.

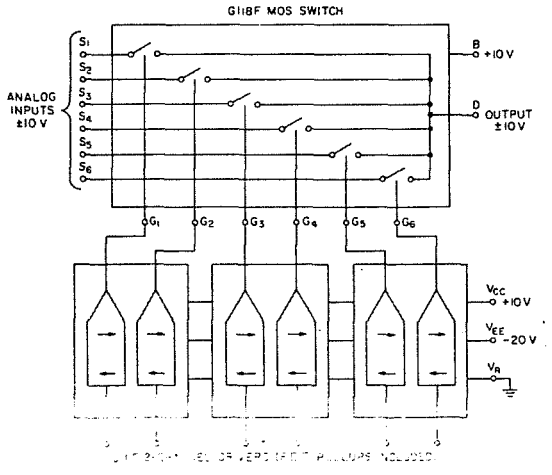
MULTIPLEXER BLOCKS



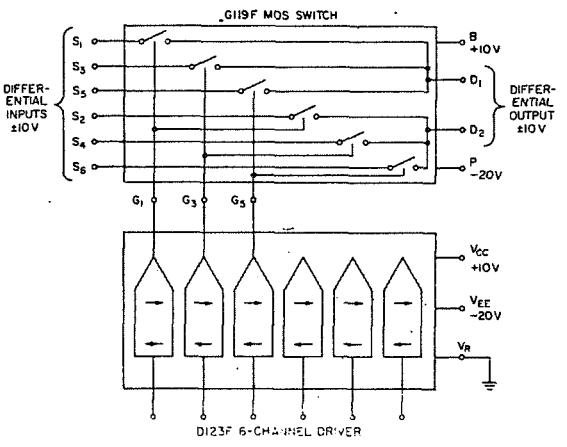
5-Channel Block



5-Channel 1st Level, 1-Channel Block



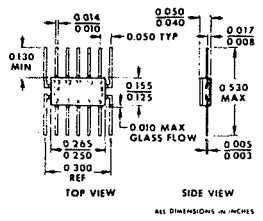
6-Channel Block



3-Channel Differential Block

P-CHANNEL, NORMALLY-OFF, TYPE C MOS FETS FOR SWITCHING APPLICATIONS

- Integrated Zener-clamp gate protection
- Integrated FET current-limiter pull-up elements supply collector current to buffer/drivers



TO-84 Flatpac
Leads: Kovar, gold-plated
Circuit substrate (V_B) is in electrical contact with the case.

These multi-channel MOS FET switches may be direct coupled to driver circuits without using isolating diodes, capacitors, or referencing resistors. The series is intended for, but not limited to, use with the Siliconix D123F buffer/driver series.

Each FET switch consists of multiple MOS FETs, integrated on a silicon chip with FET pull-up elements which provide collector loads for the driver circuits. These elements may be disabled at the user's discretion by connecting terminal P to terminal B. The drain-to-body junctions of the pull-up FETs act as Zener clamp protection on all control gates even when pull-up elements are disabled.

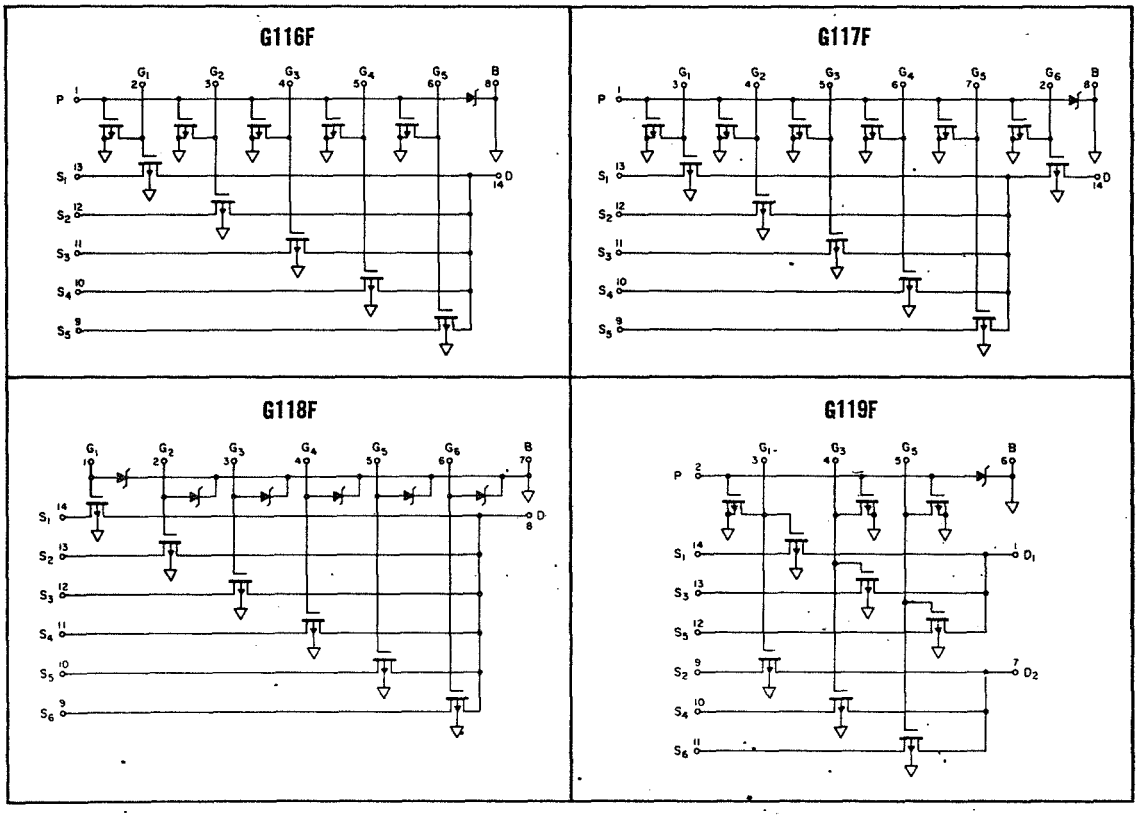
The series includes four variations accomplished by modification of metal interconnection masks. These are:

G116F A 5-channel MOS with 5 pull-up FETs, for use as a 5-channel multiplexer block.

G117F A 6-channel MOS with 6 pull-up FETs arranged as 5 input channels and 1 output channel, for use as a 5-channel 1st level and 1-channel 2nd level multiplexer block.

G118F A 6-channel MOS without pull-up FETs, for use as a 6-channel multiplexer block where the driver output pull-up elements are provided elsewhere.

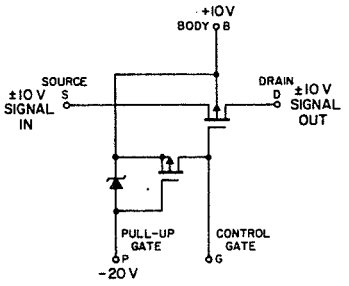
G119F A 6-channel MOS arranged in 3 pairs with 3 pull-up FETs, for use as a 3-channel differential multiplexer block.



The basic switch block for the G116F series is shown below. Terminal P of the G118F is internally connected to the body thus turning all pull-up FETs OFF; Zener protection remains in tact.

ABSOLUTE MAXIMUM RATINGS (25°C)

Body Voltage V_B to Any Terminal	-2 to +30 V
Source Current I_S	100 mA
Drain Current I_D	100 mA
Control Gate Current I_G	5 mA
Pull-Up Gate Current I_P	100 μA
Power Dissipation (Derate 3 mW/°C)	375 mW
Storage Temperature	-55 to +150°C
Operating Temperature	-55 to +125°C
(See below for alternate temperature ranges)	



ELECTRICAL CHARACTERISTICS (25°C) per channel unless otherwise noted

Characteristic		Test Conditions		Min	Max	Unit
r_{DS}	Drain-Source ON Resistance*	I_S = 100 μA,	V_{BD} = 0, V_{GD} = -30 V		125	ohm
			V_{BD} = 10 V, V_{GD} = -20 V		250	ohm
			V_{BD} = 20 V, V_{GD} = -10 V		600	ohm
$I_{S(OFF)}$	Source Cutoff Current	V_{SD} = -20 V, V_{BD} = V_{GD} = V_{PD} = 0			0.5	nA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = -20 V, V_{BS} = V_{GS} = V_{PS} = 0			0.5	nA
I_D	Drain Current (G117F only) (Total for all channels)	V_{G1B} to V_{G5B} = 0, V_{DB} = -20 V, V_{G6B} = -30 V, V_{SB} = V_{PB} = 0			3.5**	nA
$V_{GS(th)}$	Gate Threshold Voltage	I_S = -10 μA, V_{DS} = -10 V, V_{SB} = 0		-2	-6	V
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = -10 μA, V_{GS} = V_{BS} = V_{PS} = 0		-30		V
BV_{SDS}	Source-Drain Breakdown Voltage	I_S = -10 μA, V_{GD} = V_{BD} = V_{PD} = 0		-30		V
BV_{GBS}	Gate-Body Breakdown Voltage	I_G = -10 μA, V_{PB} = V_{SB} = V_{DB} = 0		-30	-90	V
BV_{PBS}	Pull-Up Gate-Body Breakdown Voltage	I_P = -10 μA, V_{GB} = V_{SB} = V_{DB} = 0		-30	-90	V
$I_{G(ON)}$	Control Gate ON Current	V_{GB} = -30 V, V_{PB} = -30 V, V_{SB} = V_{DB} = 0		-0.5	-2	mA
I_{GSS}	Control Gate Reverse Current	V_{GB} = -20 V, V_{DS} = V_{BS} = V_{PS} = 0			0.5	nA
C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance	V_{PB} = V_{GB} = V_{SB} = V_{DB} = 0, f = 1 MHz, Body Guarded			3	pF
C_{sd}	Source-Drain Capacitance				0.4	pF
C_{sb}	Source-Body Capacitance	V_{PB} = V_{GB} = V_{DB} = 0, V_{SB} = -5 V, f = 1 MHz			3.5	pF
C_{db}	Drain-Body Capacitance (Per common Drain Terminal)	V_{SB} = V_{PB} = V_{GB} = 0, V_{DB} = -5 V, V_{G6B} = -20 V (G117F only), f = 1 MHz,	G116F		18	pF
			G117F		20**	pF
			G118F		18	pF
			G119F		10	pF

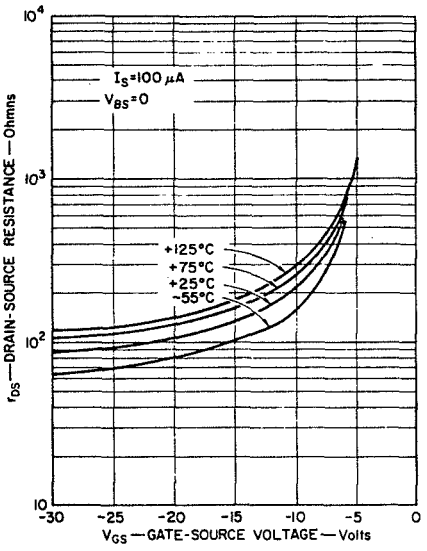
*For the G117F this is resistance from each source terminal and the drain terminal to the common internal node.
**Gate G6 (terminal 7) must be turned ON for this measurement.

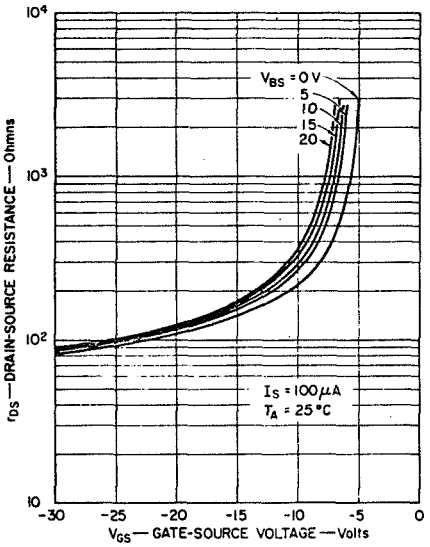
ALTERNATE TEMPERATURE RANGES

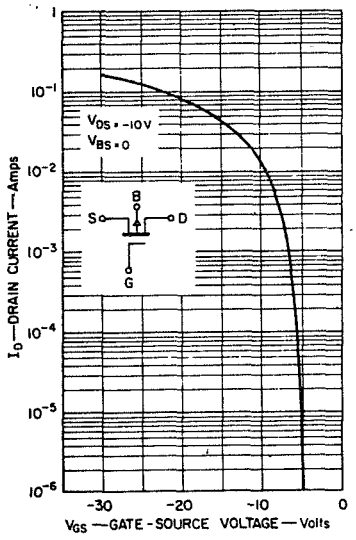
The following multiple MOS FET switches may be obtained on special order for operation at reduced temperatures:

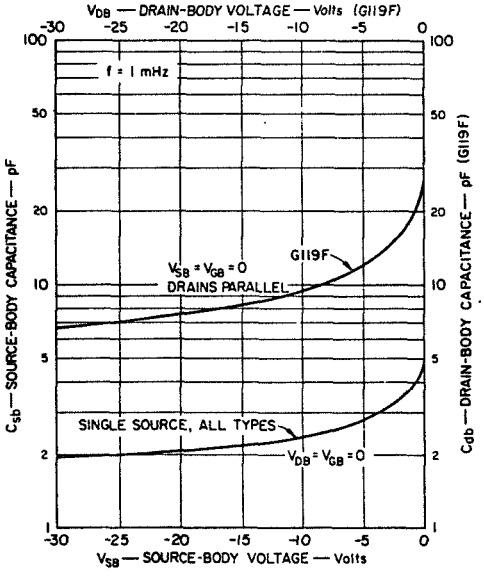
G216F Series	-55 to +85°C
G316F Series	-20 to +85°C
G416F Series	0 to +75°C

TYPICAL CHARACTERISTICS









Specifications subject to change without notice.